WAVETEK

OPERATION & MAINTENANCE MANUAL

Model 22

11 MHz Stabilized Sweep Generator

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11 MHz Stabilized Sweep Generator

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WARRANTY

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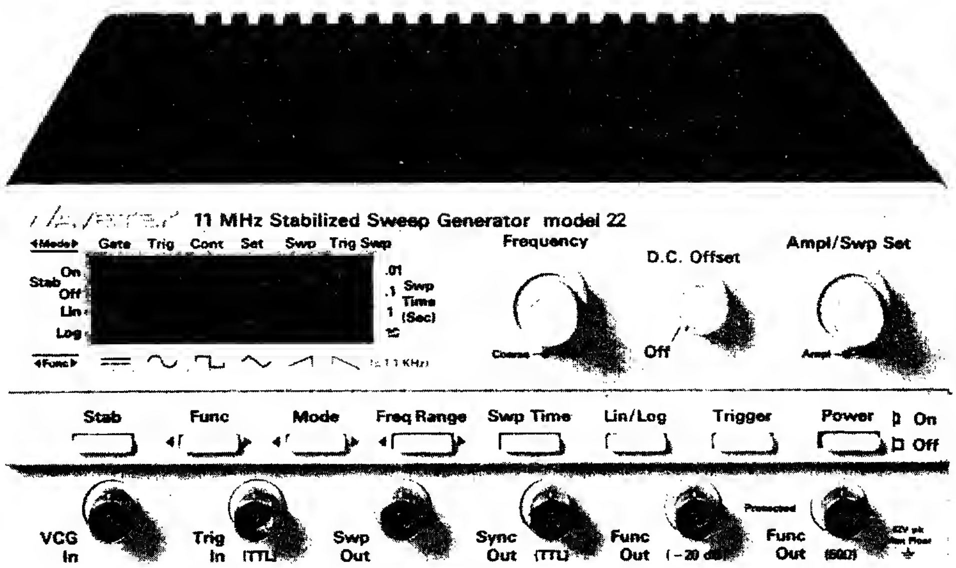
CONTENTS (Continued)

SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.



Model 22. 11 MHz Stabilized Function and Sweep Generator

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 22

Model 22 is a closed-loop, frequency stabilized, sweep/function generator. Both short term and long term frequency accuracy is 0.09% over its 100 μHz to 11 MHz frequency span.

Modes are continuous, triggered, gated, sweep set, continuous sweep and triggered sweep. Output levels are to 20V peak-to-peak (10 Vp-p into 50Ω).

Waveforms are sine, triangle, square, ramp up, ramp down, and dc. Above 1.1 kHz waveforms are analog generated; below, waveforms are digitally synthesized.

An LCD display shows frequency (3½ digits plus unit of measure) and annunciators that indicate selected operating modes, etc. The waveform output circuit is protected from accidental application of high voltage to the BNC connector.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

A bidirectional pushbutton switch selects sine (∿), triangle (∿), square (⎍) and dc (⎓), and for frequencies on or below the 1.100 kHz range, ramp up (⟋|) and ramp down (|⟍).

Operational Modes

Continuous: Generator runs continuously at selected frequency. Continuous frequency and sweep start frequency set with Frequency Course and Fine controls.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one complete waveform cycle at selected frequency.

Gated: As triggered mode, except output continues for duration of gate signal. Last waveform started is completed.

Set: Generator runs continuously at sweep stop frequency set by Sweep Set control. Sweep stop frequency is displayed.

Sweep: Generator frequency is swept from the start frequency limit set by the Frequency control to the stop frequency limit set by the Sweep Set control in a continuously occurring sweep. Sweep Time and linear or logarithmic sweep are selectable.

Triggered Sweep: Generator is quiescent until triggered by a low to high external signal at Trig In BNC or manually by Trigger button. After a trigger, generator is gated on for the duration of a single sweep at selected sweep time and start and stop frequencies. If external trigger signal has returned to the low state (or manual Trigger is released) before the end of the sweep time, generator returns to the quiescent state until the next trigger input. If trigger is high at the end of the sweep (or manual Trigger is held) the generator returns to the start frequency and runs continuously until the next trigger input.

Frequency Range

100 μHz to 11 MHz in 9 overlapping decade ranges. Range switching with bidirectional switch with frequency digits, decimal and units displayed on LCD display. Each decade range capable of 1100:1 frequency change controlled by the Frequency Course and Fine controls.

Function Output

Waveform amplitude variable over a 20 dB range up to 20 Vp-p (10 Vp-p into 50Ω) at Function Out. Waveform also present at Function Out (-20 dB) with a fixed 20 dB attenuation relative to the Function Out for a full 40 dB of amplitude range. Peak output current is 100 mA maximum at Function Out. Source impedance of both outputs is 50Ω.

DC Offset and DC Output

Waveform offset and dc output variable with DC Offset control with off position for calibrated zero offset. Function Out is ± 10V maximum (± 5V into 50Ω) as offset or Vdc output. Signal peak plus offset limited to ± 10V (± 5V into 50Ω). DC offset plus waveform attenuated proportionately at Function Out (-20 dB).

Sync Output

TTL pulse (50% duty cycle) at generator frequency. Will drive 10 LS TTL loads.

VCG — Voltage Controlled Generator

Up to 1100:1 frequency change with external 0 to ±5V signal applied to VCG IN connector. Upper and lower frequencies limited to maximum and minimum of selected range. Input impedance is 5kΩ and maximum slew rate is 0.1V/μs. VCG IN is disconnected when the Stabilizer is enabled.

Trigger and Gate

External TTL compatible signal at Trig In BNC triggers or gates generator output when generator is in trigger, gate or triggered sweep mode. Generator triggers on positive edge of input or gates on for duration of high level input. External signal pulse width is 50 ns minimum with a maximum repetition rate of 5 MHz.

Stabilizer

When selected, the generator frequency is stabilized at the displayed frequency to a crystal-controlled reference.

When the stabilizer is on, long term frequency stability is corrected to the displayed frequency over the entire operating temperature range of 0 to +50°C. The stabilizer is automatically turned off when the mode is taken out of continuous or when Log frequency is enabled.

Display

1100 count LCD frequency display with frequency ranging units (mHz, Hz, kHz, and MHz) and a floating decimal point. Annunciators indicate selection of waveform, stabilizer status, generator mode, sweep time and linear or logarithmic sweep.

Sweep Generator

Sweep Mode: Linear or logarithmic, up to 3 decades.

Sweep Time: Selectable (in seconds) .01, .1, 1 and 10.

Sweep Output: Output voltage at sweep out connector proportional to the sum of Frequency control, internal sweep voltage and external VCG In voltage. Scale factor is 0 to +5V (open circuit) linear voltage change from bottom to top frequency of a range. Source impedance is 600Ω for driving horizontal axis of oscilloscope or recording equipment.

Sweep Width: Up to 1100:1 linear or logarithmic.

1.2.2 Frequency Precision

Frequency Display Accuracy

±1 count of 1100 counts, which is 0.09% of range. Stabilizer maintains same reading indefinitely.

Time Symmetry

Square waveform variation from 1100 to 100 counts on display less than:

±1% to 110.0 kHz,
±5% to 11.00 MHz.

1.2.3 Amplitude Precision

Sine Variation with Frequency

Less than:
±0.2 dB on all ranges up through the 110.0 kHz range,
±1.5 dB to 11.00 MHz.
Referenced to 1 kHz.

1.2.4 Waveform Characteristics

Sine Distortion

<0.5% THD up through the 11.00 kHz range.
<1.0% THD on 110.0 kHz range.

All harmonics 40 dB below fundamental on 1.100 MHz range, and 28 dB below fundamental on 11.00 MHz range.

Square Wave

Rise/Fall Time: <22 ns

Total Aberrations: Each peak <5% of p-p amplitude.

Triangle Linearity

>99% to 110.0 kHz.

1.2.5 General

Output Protection

Function outputs are protected against a short circuit to any voltage between ±10V dc and also have internal fused protection (both output and common conductors) against accidental application of up to 250 Vac or 350V dc.

Stability

Amplitude, Frequency (Non-Stabilized) and DC Offset:

After 30 minute warm-up:
±0.10% of range for 10 minutes,
±0.50% of range for 24 hours.

Frequency (Stabilized): ±0.10% of range for ⩾10 minutes, 0 to 50°C.

Environmental

Temperature Range: 25°C ± 10°C for spec. operation, operates 0°C to 50°C, -20°C to +75°C storage.

Warm-up Time: 40 minutes for specified operation.

Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.

Relative Humidity: 95% at 25°C and at sea level (noncondensing).

Dimensions

21.1 cm (8.3 in.) wide, 8.6 cm (3.4 in.) high, 30.5 cm (12 in.) deep.

Weight

3.4 kg (7 1/2 lb) net, 4.5 kg (10 lb) shipping.

Power

90 to 128, 180 to 256V, 48 to 66 Hz, less than 35 VA.

NOTE

All specifications apply for display between 1100 and 100 frequency counts; amplitude at 10 Vp-p into 50Ω.

SECTION 2
INITIAL PREPARATION

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage. If damage is discovered, file a claim with the carrier who transported the instrument. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 3/8 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit.

2.2.2 Verifying the Line Voltage

CAUTION

All calibration pots are located inside the bottom cover on the circuit board. Be careful not to bump any pots, as this may require a recalibration of the instrument. Moving R103, located near the front panel, can keep the generator from operating; if adjustment is needed, refer to table 5-1 steps 1 through 10.

To verify the line voltage (or change the fuse), the operator must first remove the top and bottom covers. Remove the top and bottom using the following steps and figure 2-1.

1. Remove two (2) screws holding top and bottom covers to rear panel.
2. Slide both covers (together as a unit) to the rear and remove from the chassis assembly.

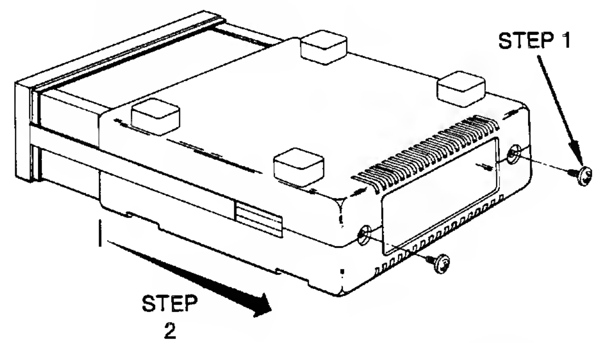


Figure 2-1. Top and Bottom Cover Removal

After the covers have been removed, the line voltage can be checked by viewing the voltage label through the inspection hole as shown in figure 2-2.

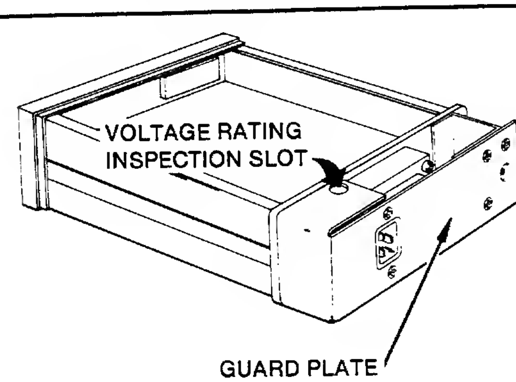


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct, perform the following steps and refer to figure 2-3 for step 1, and figure 2-4 for steps 2 thru 4 to change the line voltage and fuse.

1. Remove the two screws attaching the fuse cover to the guard plate.

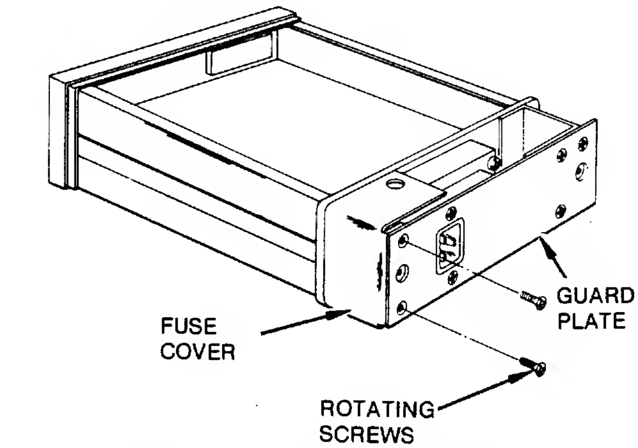


Figure 2-3. Guard Plate Removal

2. Remove the voltage selector connector from the ac primary board. Rotate the connector until the correct voltage selector indicator is on top.

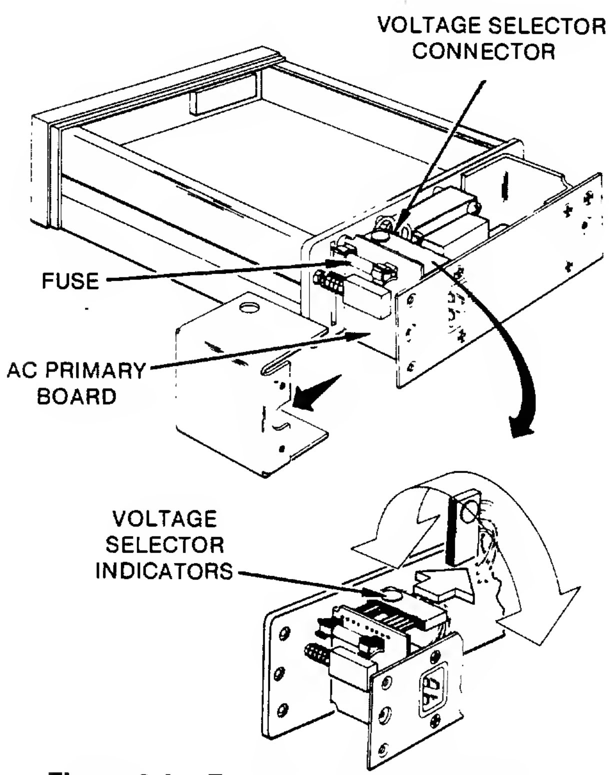


Figure 2-4. Fuse and Voltage Selection

3. Reinstall the voltage selector connector.
4. Remove the fuse and install new fuse as called out in table 2-1.

Table 2-1. Voltage/Fuse Selection

Connector Position	Voltage Range	Fuse
115V	90 to 128 Vac	3/8 amp
220V	180 to 256 Vac	3/16 amp

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the fuse cover is attached to the unit.

2.2.4 Reassembly

Refer to figure 2-3 for step 1 and figure 2-5 for steps 2 thru 4.

1. Fasten the fuse cover to the guard plate with the two screws.

CAUTION

When sliding on the bottom cover, avoid pinching any coaxial cables located near the front panel.

2. Turn the instrument upside down, position the bottom cover over the guard shield, and then slide the bottom cover forward approximately two inches while engaging the cover and slides (see figure 2-5, detail A and detail B). Don't slide the cover on yet.
3. Turn the instrument right side up. Install the top cover using the same procedure as in step 2. Don't slide the cover on yet.
4. Align the rear of both the top and bottom cover with each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly together and slide the chassis assembly into the mated top and bottom covers.
5. Secure covers to the chassis assembly using two screws as shown in figure 2-1.

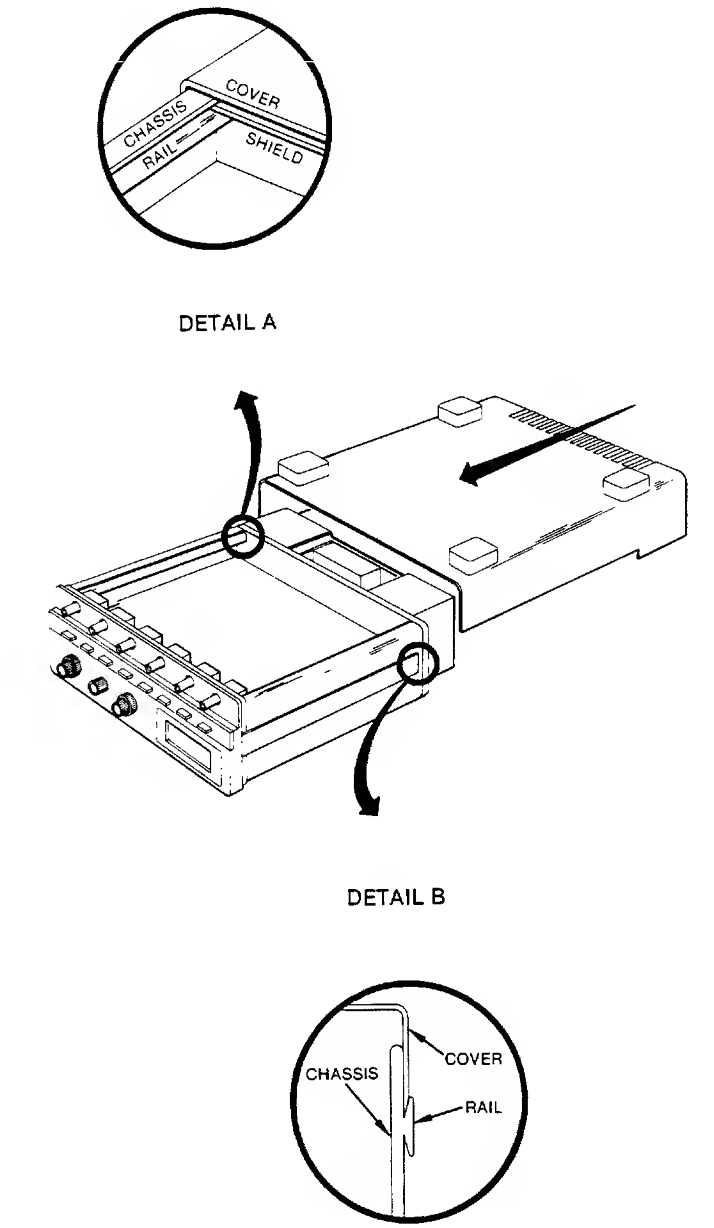


Figure 2-5. Top and Bottom Cover Installation

2.2.5 Signal Connections

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

NOTE

Signal ground may be floated up to ± 42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.3 INITIAL CHECKOUT PROCEDURE

The initial checkout procedure in table 2-2 allows the operator to learn the basic operation and capabilities of the Model 22 in an easy and orderly fashion. In addition, it can be used as a receiving inspection or post-repair checkout. While this procedure verifies functional operation of this instrument, it does not verify the calibration. **The frequencies shown are typical values and should only be used as a guide.** Required tools and test equipment are listed below.

Instrument	Comments
Oscilloscope	Dual channel, 100 MHz bandwidth
Voltage Source	+ 5Vdc
50Ω Feedthrough	0.5% accuracy, 2W
External Generator	200 Hz to 1.1 MHz TTL output
BNC Tee	1 male, 2 female connector
BNC Coax Cable	RG58U, 3 ft. length (3 each)

2.3.1 Using the Procedure

The checkout procedure (table 2-2) can be used several different ways. It can be started at step 1 and followed straight through to the final step. Or, it can be entered at the highlighted steps, which start specific groups of checks. If the table is being followed in sequence from the previous step, perform the instructions as written. But if starting at a highlighted step, the Model 22 must first be reset to the power on settings (see below). To do this, turn the Power Off, then On.

Power-On status:

Frequency Range: 0.001 to 1.100 kHz
Mode: Continuous
Function: Sine
Lin/Log: Lin
Sweep Time: 0.01s.
Stabilizer: Off

2.3.2 Front Panel Switches

The Func, Mode, and Freq Range switches are bidirectional. To use these switches, the operator must press the left or right side of the switch's front surface, as indicated by the arrows on the panel. Pressing the center of any bidirectional switch does not ensure correct operation. All other switches can be pressed anywhere.

When a switch is pressed, either the frequency or an annunciator on the display will change, as shown in table 2-2.

Table 2-2. Initial Checkout Procedure

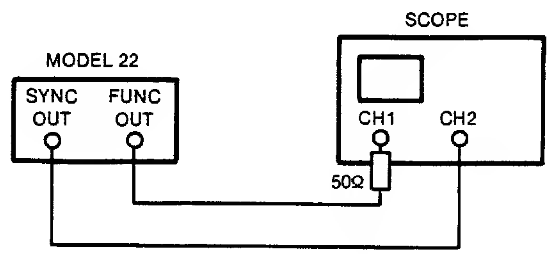
NOTE

1. *Before beginning this procedure, review paragraph 2.3.*
2. *Frequencies shown are typical and should only be used as a guide.*
3. *If starting at a highlighted step, first press Power Off, then On.*

Initial Settings

Control	**Setting**
Frequency	
Coarse	cw
Fine	cw
D.C. Offset	Off
Amplitude	cw
Swp Set	cw

Test Setup 1



Scope	**Setting**
Time base	0.2 ms/div
CH1 Vert	2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

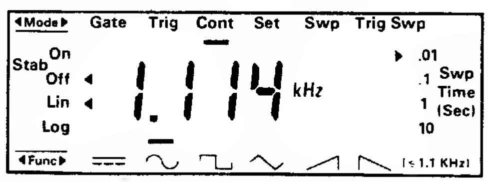
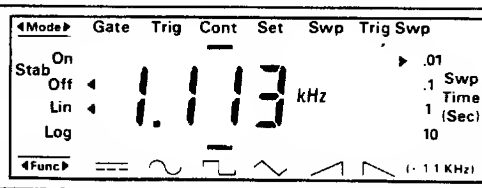
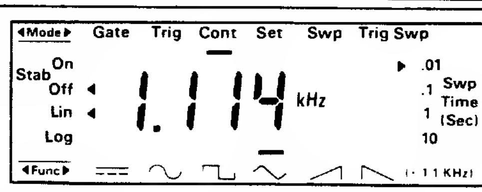
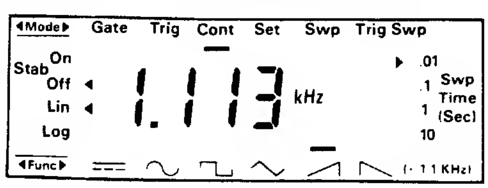
Step	**Control**	**Operation**	**Display**	**Observation/Comments**
Function Check				
1	Set to Initial Settings Power On			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
2(a)	Func	Press Once		10Vp-p square wave.
2(b)		Press Once		10Vp-p triangle.
2(c)		Press Once		10Vp-p ramp up.

Table 2-2. Initial Checkout Procedure (Continued)

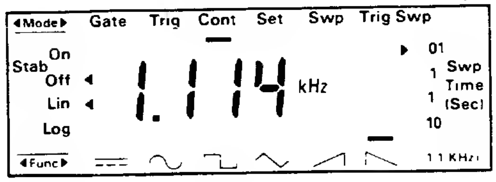
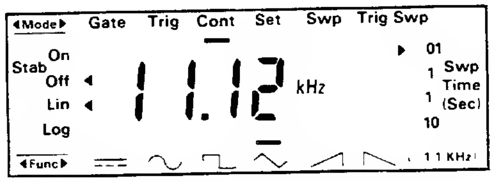
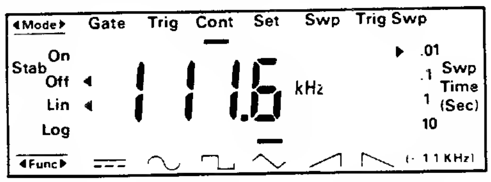
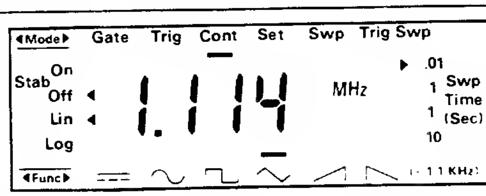
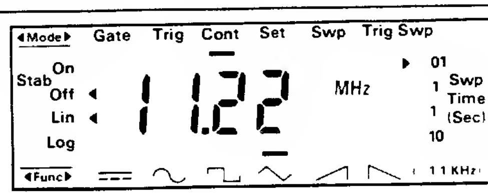
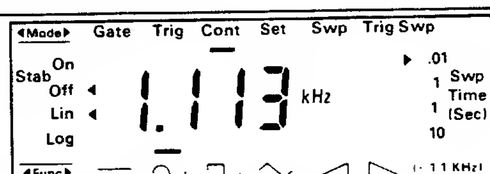
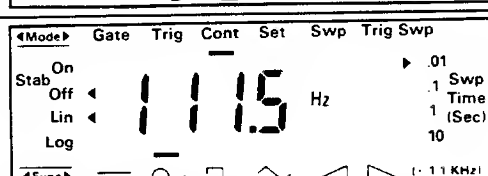
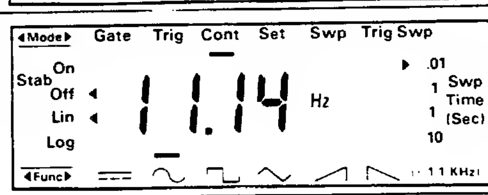
Step	Control	Operation	Display	Observation/Comments
2(d)	Func	Press Once		10Vp-p ramp down
Frequency Range Check (11k to 11 MHz)				
3(a)	Freq Range	Press Once		11 kHz, 10Vp-p triangle. Ramp defaults to triangle above the 1.1 kHz range.
3(b)		Press Once		110 kHz
3(c)		Press Once		1.1 MHz
3(d)		Press Once		11 MHz
Frequency Range Check (110 Hz to 110 mHz)				
4	Set to Initial Setting			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off then to On.		
5(a)	Freq Range	Press Once		110 Hz
5(b)		Press Once		11 Hz

Table 2-2. Initial Checkout Procedure (Continued)

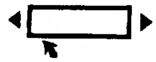
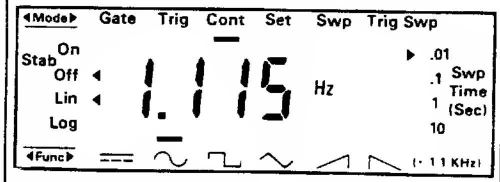
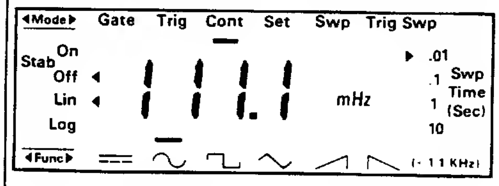
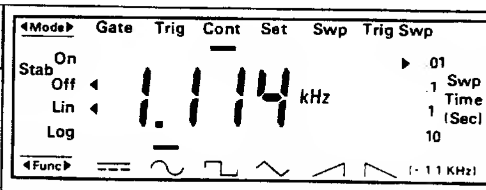
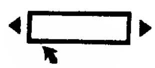
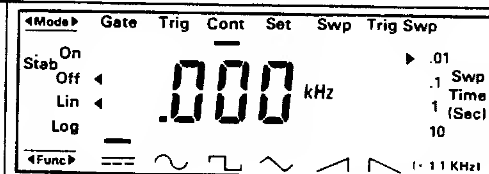
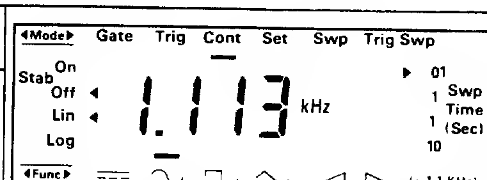
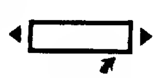
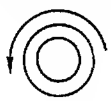
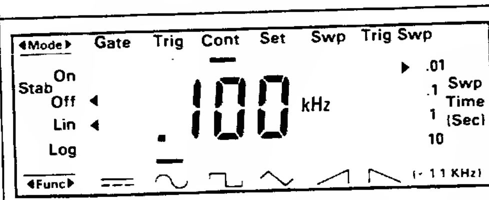
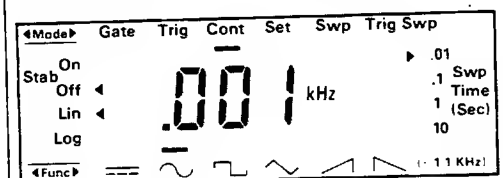
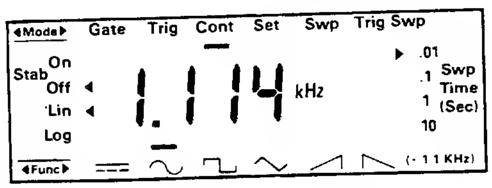
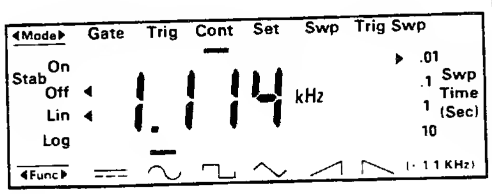
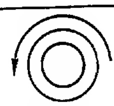
Step	Control	Operation	Display	Observation/Comments
5(c)	Freq Range	 Press Once		1.1 Hz
5(d)		 Press Once		110 mHz
DC Offset Check				
6	Set to Initial Setting			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off then to On.		
7	Func	 Press Once		0 Vdc
8(a)	D.C. Offset	 Full cw		Greater than +5 Vdc
8(b)		 Full ccw, but not off		Greater than −5 Vdc
8(c)		 Off		0 Vdc
Coarse and Fine Frequency Check				
9	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Func	 Press Once		

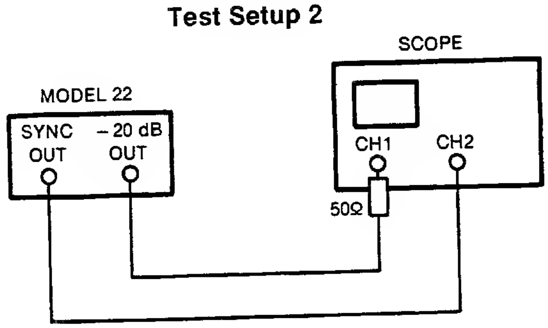
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
10	Frequency Coarse	 Full ccw		Approximately 11:1 frequency change. Verify all display segments function.
11	Frequency Fine	 Full ccw		Approximately 100:1 frequency change.
12	Frequency Coarse and Fine	 Both full cw		Total frequency change of 1100:1.

Amplitude Check

Step	Control	Operation	Display	Observation/Comments
13 (a)	Set to Initial Setting			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave; output level decreases to 1 Vp-p as control is rotated.
	Amplitude	 Full ccw		

Test Setup 2

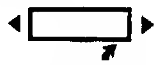
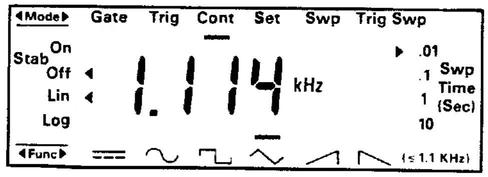
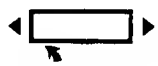
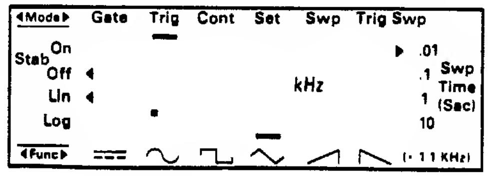


Step	Control	Operation	Display	Observation/Comments
13(b)		 Rotate cw		Connect as shown in test setup 2. Output increases from 0.1 to 1 Vp-p.

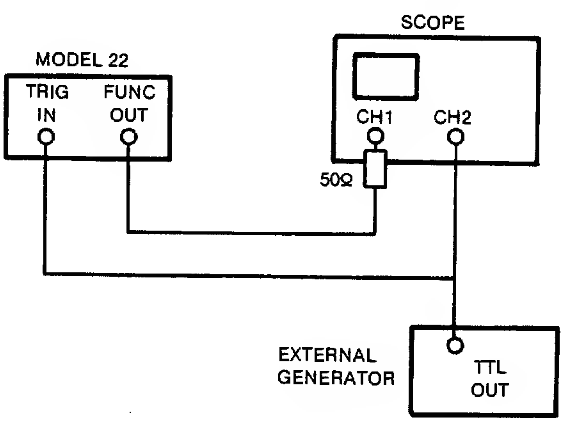
Sync Out Check

Step	Control	Operation	Display	Observation/Comments
14				Display CH2; 1.1 kHz TTL square wave.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
Trigger and Gated Check				
15	Set to Initial Settings			
	Func	 Press Twice		Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p triangle.
16(a)	Mode	 Press Once		Approximately 0 Vdc level.

Test Setup 3



Scope	Settings
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH2
Display	CH1 and CH2

External Generator Setting
200 Hz TTL

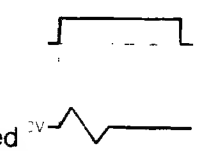
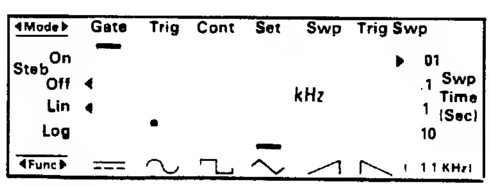
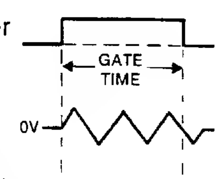
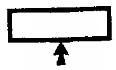
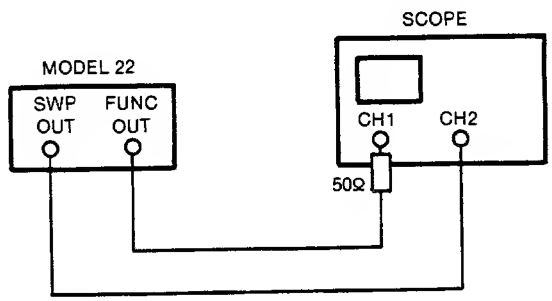
Step	Control	Operation	Display	Observation/Comments
16(b)		Connect as shown in test setup 3		CH2: Trigger Input / CH1: Triggered Triangle 
16(c)		 Press Once		CH1: Trigger Input / CH2: Gated Triangle 
16(d)	Trig In	Disconnect External Generator		Display CH1. 0 Vdc.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
Manual Trigger Check				
17	Trigger	 Press and Hold		Continuous triangle while trigger button is pressed.
Sweep Check				

Test Setup 4



Scope	Settings
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH1
Display	CH1 and CH2

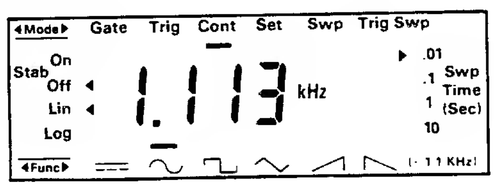
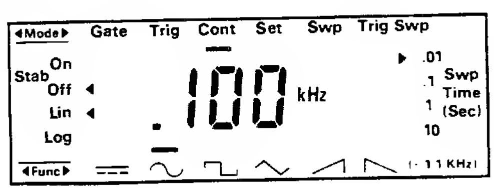
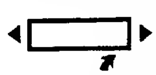
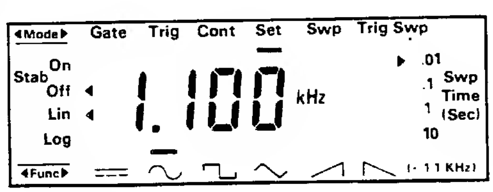
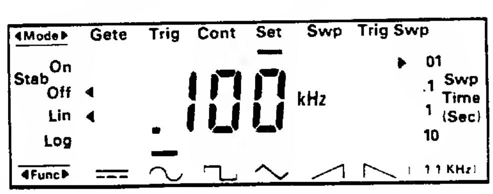
Step	Control	Operation	Display	Observation/Comments
18	Set to Initial Settings Power	Press to Off then to On		Connect as shown in test setup 4 CH1: 1.1 kHz 10 Vp-p sine wave. CH2: +5 Vdc level.
19	Frequency Coarse	 Full ccw		CH1: 100 Hz sine wave. CH2: Voltage level decreases.
20	Mode	 Press Once		CH1: 1.1 kHz sine wave. CH2: +5 Vdc level.
21(a)	Swp Set	 Full ccw		CH1: 100 Hz sine wave. CH2: Voltage level decreases.

Table 2-2. **Initial Checkout Procedure (Continued)**

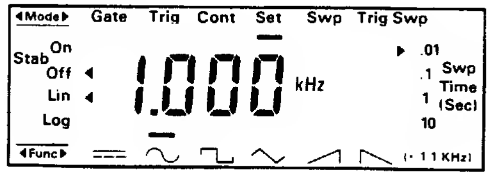
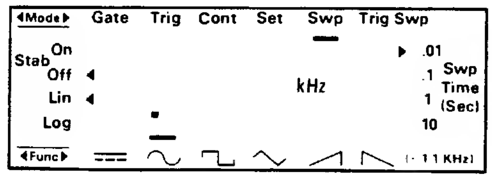
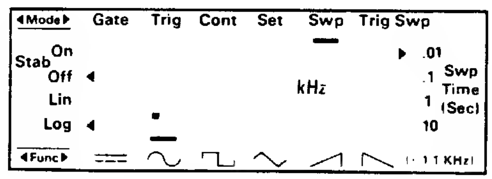
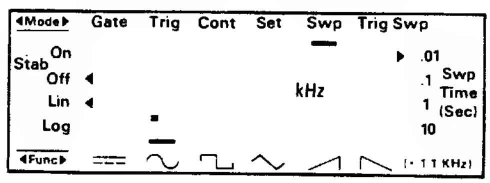
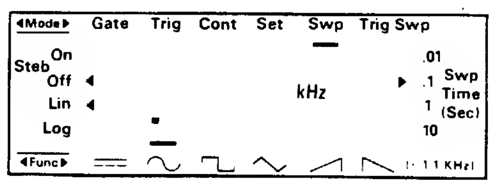
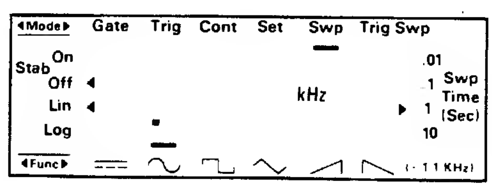
Step	Control	Operation	Display	Observation/Comments
21(b)	Swp Set	See comments		Display: Set to 1.00 kHz. CH1: 1.00 kHz sine wave. CH2: Voltage level decreases.
22	Mode	Press Once		Trigger scope on falling edge of sweep range (CH2). CH1: Linear sine wave sweep from 100 Hz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).
23(a)	Lin/Log	Press Once		Logarithmic sine wave sweep from 100 Hz to 1.00 kHz.
23(b)		Press Once		Linear sine wave sweep from 100 Hz to 1.00 kHz.
24(a)	Swp Time	Press Once		Scope: Trigger sweep to normal; time base to 10 ms/div. CH1: Linear sine wave sweep from 100 kHz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).
24(b)		Press Once		Scope: Time base to 0.1 s/div. CH1: Linear sine wave sweep from 100 Hz to 1.00 kHz. CH2: Ramp up (10 divisions on scope).

Table 2-2. Initial Checkout Procedure (Continued)

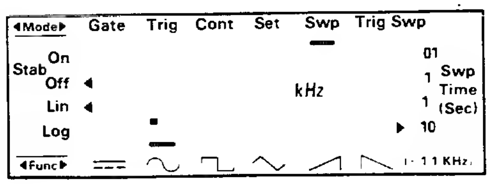
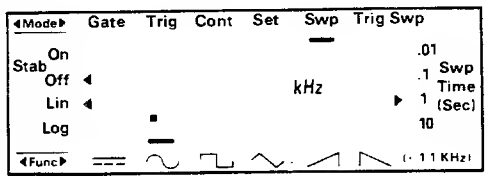
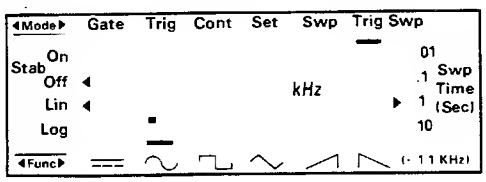
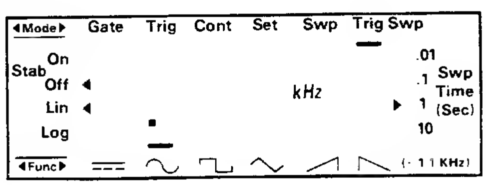
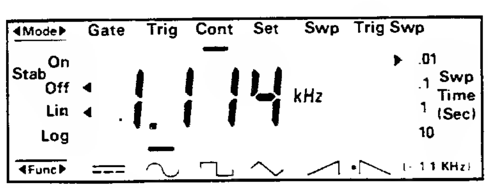
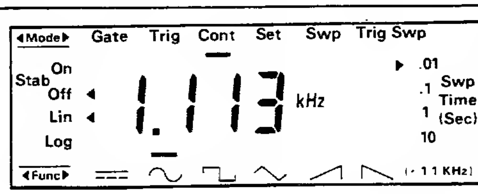
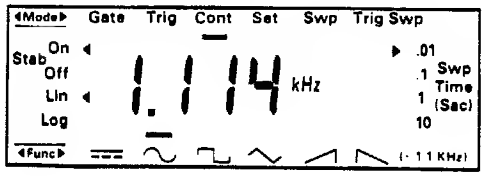
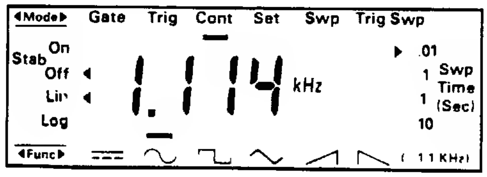
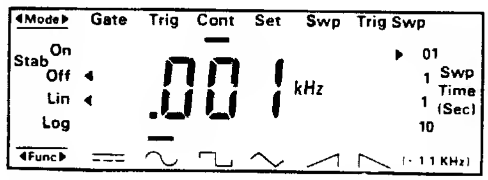
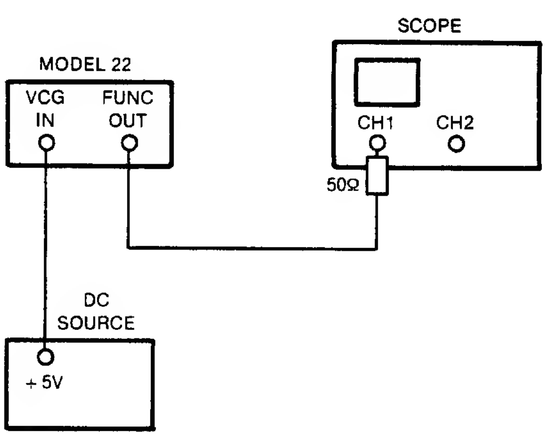
Step	Control	Operation	Display	Observation/Comments
24(c)		Press Once		Scope: Time base to 1 ms/div. CH1: Linear sine wave sweep from 100 Hz to 1.00 kHz. CH2: Slow rising ramp.
24(d)		Press three times		Scope: Time base to 1s/div. Sweep time annunciator steps to 0.01 ms, 0.1 s to 1 s each time the switch is pressed.
25	Mode	Press Once		CH1: 0 Vdc level.
26(a)	Trigger	Press and release		CH1: Triggered sine wave sweep from 100 Hz to 1.00 kHz in 1s and return to quiescent 0V level.
26(b)		Press and Hold		Triggered sine wave sweep from 100 Hz to 1.00 kHz in 1s and returns to 100 Hz.
Stabilizer Check				
27	Set to Initial settings			Connect generator as shown in test setup 1. 1.1 kHz 10 Vp-p sine wave.
	Power	Press to Off then to On		
28	Frequency Fine	See Comments		Rotate knob until the least significant digit fluctuates between two digits.

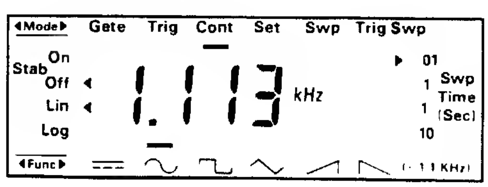
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
29	Stab	Press Once		The least significant digit remains stabilized.
VCG Check				
30	Set to Initial Settings			
	Stab	Press Once		1.1 kHz 10 Vp-p sine wave.
31	Frequency Coarse and Fine	Both full ccw		Low frequency sine wave.

Test Setup 5



Scope	Settings
Time base	0.2 ms/div
CH1 Vert	2 V/div
Display	CH1

Step	Control	Operation	Display	Observation/Comments
32	VCG In	+ 5 Vdc		Connect as shown in test setup 5. 1.1 kHz 10 Vp-p sine wave.

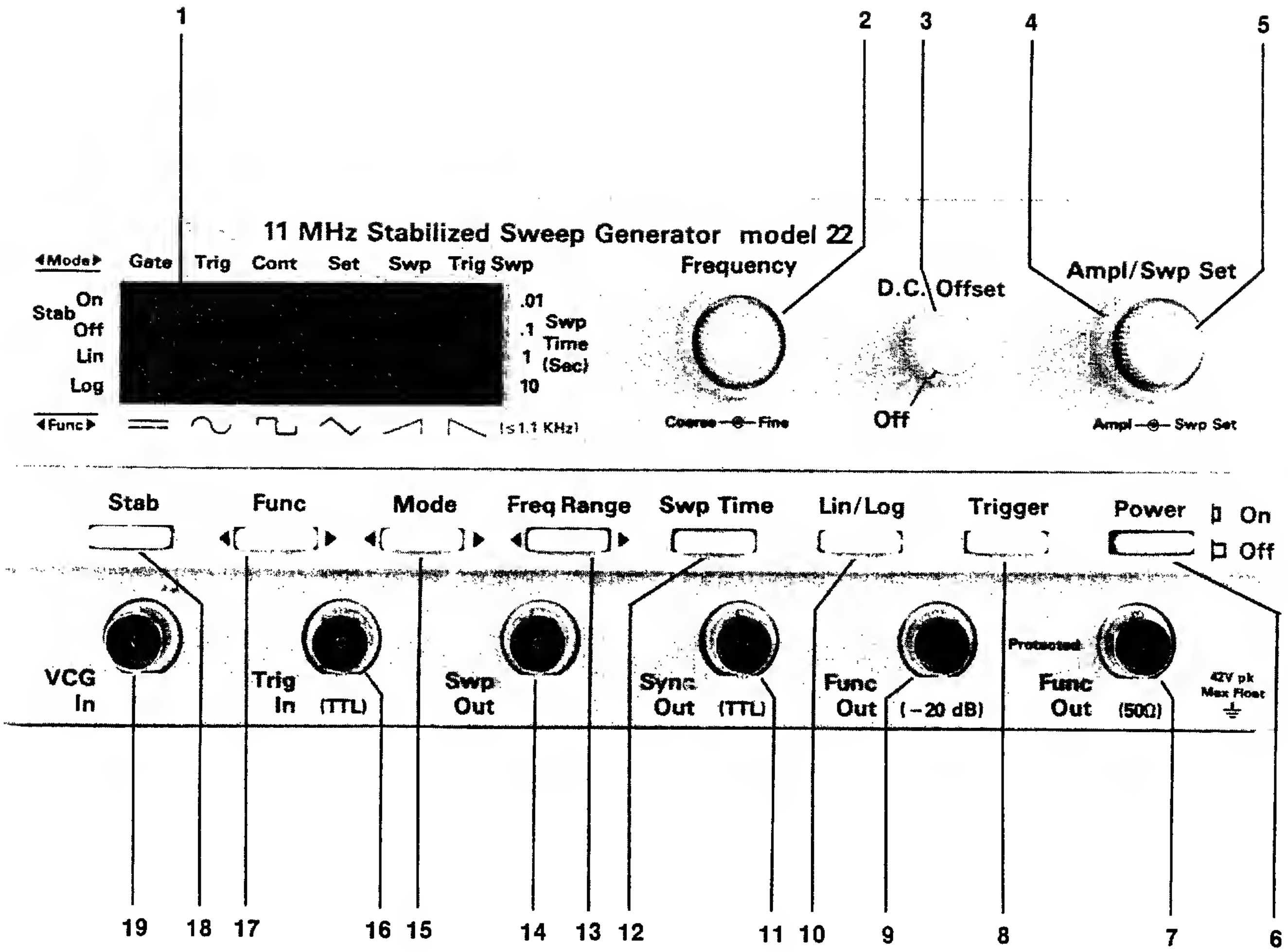


Figure 3-1. Controls and Connectors

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes the operation of the Model 22. The first part describes the controls and connectors of the instrument. The following part illustrates several applications which use the various functions and modes of this instrument.

3.2 CONTROLS AND CONNECTORS

Figure 3-1 shows the front panel controls and connectors that are keyed to the following paragraphs.

1 **Display** A 3½ digit (1100 count) LCD frequency display which incorporates annunciators that indicate Mode, Function (waveform), stabilizer on/off, lin/log sweep, and sweep time.

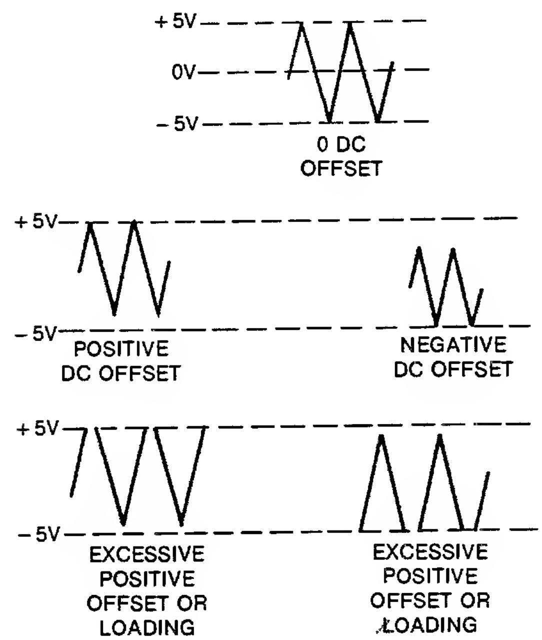
2 **Frequency Controls** The coarse frequency control, the outer knob of the concentric pair, allows coarse frequency adjustment (approximately 1000 counts) within the selected frequency range.

The fine frequency control, the inner knob of the concentric pair, allows fine frequency adjustment (approximately 100 counts) within the selected frequency range.

For linear mode, these controls vary the frequency linearly over the frequency range. For logarithmic mode, these controls vary the frequency logarithmically over the frequency range. Together the fine and coarse controls cover a 1100:1 frequency span within a selected range.

3 **D.C. Offset Control** The DC offset knob controls the dc voltage and offset of waveforms. A clockwise rotation vertically offsets the waveform up from the normal position (figure 3-2). A counterclockwise rotation vertically offsets the waveform down from the normal position (figure 3-2). A full counterclockwise rotation to Off ensures zero offset.

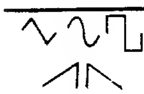
4 **Amplitude Control** The amplitude knob, the outer knob of the concentric pair, controls waveform amplitudes. Rotate the control full clockwise for maximum amplitude (see table 3-1). A counterclockwise rotation decreases the amplitude by 20 dB.



Function Out (50Ω) terminated with 50Ω

Figure 3-2. DC Offset Control

Table 3-1. Maximum Voltage

Function	Open Circuit	50Ω Termination
	20 Vp-p	10 Vp-p
DC	±10V	±5V

5 **Sweep Set Control** The Swp Set control, the inner knob of the concentric pair, sets the stop frequency in the sweep modes (see figure 3-3).

6 **Power Switch** The power switch turns the instrument On or Off. At power-up the instrument initializes in the following conditions:

Stab: Off
Func: Sine
Mode: Cont
Freq Range: 0.001 to 1.100 kHz
Lin/Log: Lin
Swp Time: 0.01s

7 **Function Output Connector** This BNC connector is the main output for the selected function. The Amplitude knob **4** controls the amplitude from 1 to 10 Vp-p into a 50Ω load (20 Vp-p into open circuit). Source impedance is 50Ω **and is internally fuse protected against accidental aplication to high voltage.**

8 **Trigger Switch** In triggered mode, the trigger button, when pressed, manually initiates a single cycle of the selected waveform. In the gated mode, it gates the output until the button is released; the last gated cycle will always be completed. The quiescent output depends on the waveform selection and dc offset (see figure 3-4). In triggered sweep mode, the trigger button, when pressed, initiates a triggered sweep (refer to Triggered Sweep Mode).

9 **Function Output (−20dB)** This BNC connector is the same as the Func Out **7** except the output is 1/10th (−20dB) of the amplitude, 0.1 to 1Vp-p. Both the waveform and offset are attenuated at Func Out (-20 dB). Source impedance is 50Ω **and is internally fuse protected against accidental application to high voltage.**

10 **Lin/Log Switch** When pressed, the Lin/Log switch selects either linear or logarithmic mode for up to 1100:1 linear or logarithmic frequency range. An annunciator arrow on the display indicates the status.

11 **Sync Output** This output is a TTL square wave at the frequency of the generator. This output can be used as a synchronizing reference for the Function Outputs **7** and **9**. Phase of the waveforms relative to the sync output is shown in figure 3-4.

12 **Sweep Time Switch** The Sweep time button, when pushed, steps through the sweep time (.01, .1, 1, and 10 seconds). Sweep time is indicated by an annunciator arrow on the display. Frequency of the internal sweep ramp, the sweep rate, is governed by the Sweep time switch **12** (see figure 3-3).

13 **Frequency Range Switch** Frequency Range switch, when pushed on the left or right, steps through the nine frequency ranges, a shown below.

Specified Range	Lowest Obtainable Frequency
11.00 to 1.00 MHz	0.01 MHz
1.100 to 0.100 MHz	0.001 MHz
110.0 to 10.0 kHz	0.1 kHz
11.00 to 1.00 kHz	0.01 kHz
1.100 to 0.100 kHz	0.001 kHz
110.0 to 10.0 Hz	0.1 Hz
11.00 to 1.00 Hz	0.01 Hz
1.100 to 0.100 Hz	0.001 Hz
110.0 to 10.00 mHz	0.1 mHz

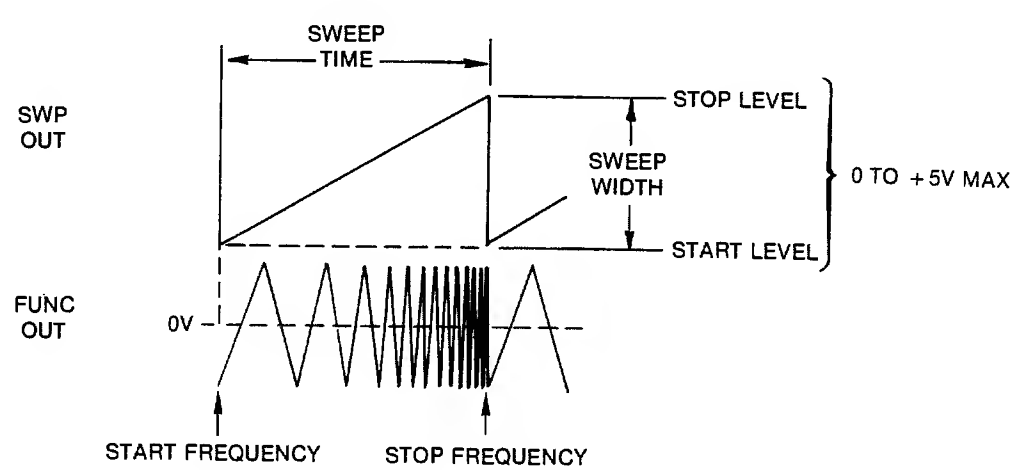


Figure 3-3. Sweep Time and Width

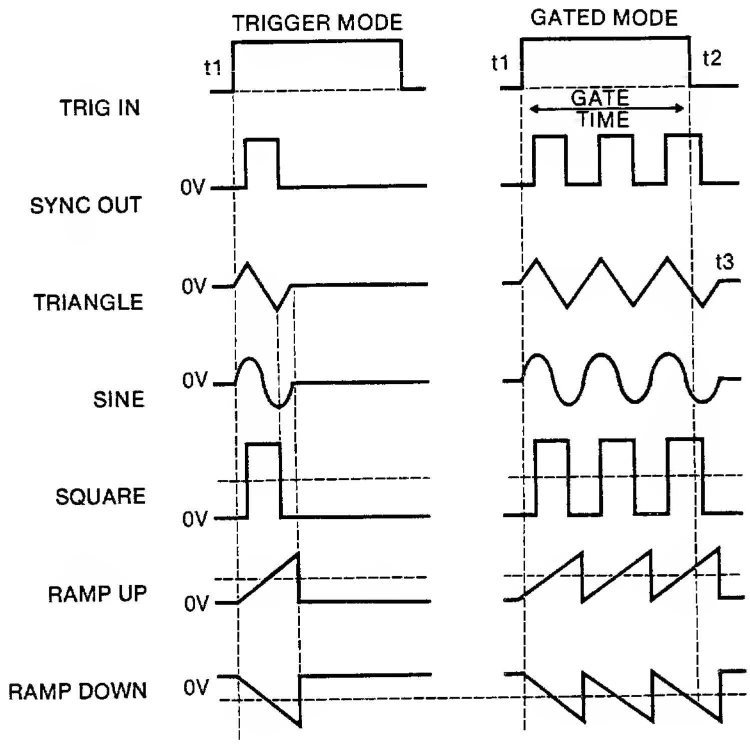


Figure 3-4. Waveform Phase Relationships

the LCD display **1**. Each range has an 1100:1 breadth. Power-up range is 0.100 to 1.100 kHz.

14 **Sweep Out Connector** The Swp Out BNC provides a linear ramp at the frequency selected by the Swp Time **12** switch. The ramp will be linear in both linear and logarithmic modes. The output voltage is proportional to the linear output frequency which is a summation of Frequency knobs **2** position, internal sweep voltage and external voltage at VCG In **18** connector. Output source impedance is 600Ω.

15 **Mode Switch** The Mode switch, when pushed on the left or right, steps through the six operating modes of the instrument.

Continuous (CONT) Generator runs continuously at the selected frequency. This is also the sweep start frequency.

Triggered (TRIG) Generator is quiescent (quiescent level depends on waveform and offset selected, figure 3-4) until triggered, at which time one complete cycle of waveform is generated.

Gated (GATE) As for triggered except the waveform is continuous for the duration of the gate signal. When the signal stops, the last waveform cycle started is completed.

Sweep Set (SET) The generator runs continuously at the sweep stop frequency set by Swp Set **5** knob. The sweep stop frequency is displayed.

Continuous Sweep (SWP) The generator frequency sweeps from the start frequency limit, set by the frequency knobs **2**, to the stop limit, set by the Swp set **5** knob.

Triggered Sweep (TRG SWP) The generator is quiescent until triggered by a low to high external signal at Trig In or by the Trigger button. After receiving this trigger, the generator makes a single sweep at the selected sweep time start and stop frequencies. If the trigger signal is low at the end of a sweep, the generator returns to the quiescent

state. If the trigger is high at the end of a sweep, the generator returns to the start frequency and runs continuously until the next trigger pulse.

For proper operation, repetition rate of the trigger pulse should not exceed twice the sweep time.

An annunciator on the display indicates the selected mode.

16 **Trigger In Connector** The Trig In connector accepts a positive-going TTL level input (t_1) to trigger and gate the generator, as shown in figure 3-4. A negative-going edge (t_2) ends the gated operation. When triggered, the generator produces one complete cycle for each trigger input. When gated, the generator produces continuous cycles until the gate signal (t_2) is removed; the last cycle started is always completed (t_3).

17 **Function Switch** The Func switch, when pushed on the left or right, steps through the six function of the Model 22: sine ∿ , triangle ∧∨ , square ⊓⊔ , ramp up ⟋| , ramp down |⟍ , and dc. An annunciator on the LCD display **1** indicates the selected function. Ramps are only available at frequencies at or below the 1.100 kHz range.

18 **VCG In Connector** This connector accepts 0 to ± 5V ac or dc input signals, which, when summed with a level proportional to the frequency knobs setting, controls the output frequency within the selected range. Positive input levels increase the frequency, while negative inputs decrease the frequency. Frequency excursions of 1100:1 are possible by placing the Frequency knobs **2** to full clockwise (0 to − 5V) or counterclockwise (0 to + 5V). Input impedance is 5kΩ. VCG slew rate is 0.1V/μs. If frequency stabilization is selected, the VCG In connector is internally disconnected.

19 **Stabilizer Switch** The Stab button references the generator to an internal standard which maintains the frequency within ± 1 (least significant) digit. An annunciator on the LCD display **1** indicates the status of the stabilizer. The stabilizer works only in the continuous mode and with an internal reference.

3.3 OPERATION

Perform the initial checkout procedure in Section 2 for a feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.2. Bold numbers are keyed to figure 3-1. Outputs are shown in figure 3-4.

3.3.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, figure 3-5 shows proper termination of the Func Out (50Ω) connector. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

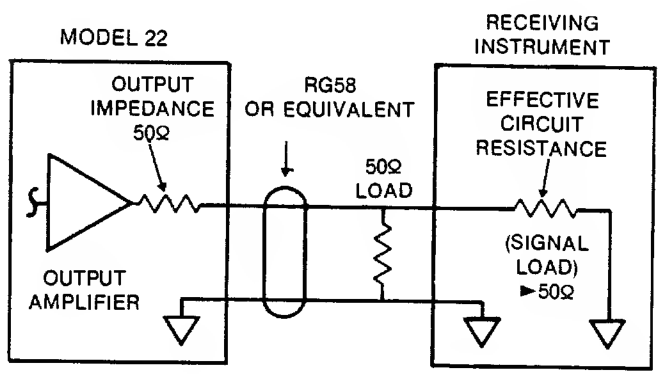


Figure 3-5. Signal Termination

The input and output impedances of the generator connectors are:

Connectors	Impedance
Func Out (50Ω) **7**	50Ω
Func Out (− 20 dB) **9**	50Ω
Sync Out **11**	TTL
Swp Out **14**	600Ω
Trig In **16**	TTL
VCG In **18**	5kΩ

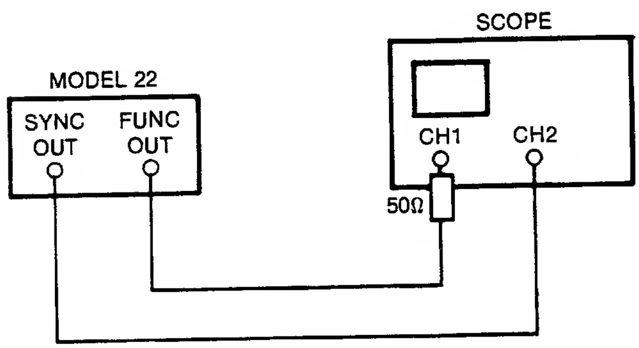
3.3.2 Continuous Operation

The basic generator supplies a continuous function (waveform) at a fixed frequency set by the operator.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **15**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).

Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate continuous operation connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	**Scope Settings**
Power: On	Time base: 0.2 ms/div.
Amplitude: cw	CH1 Vert: 2V/div
D.C. Offset: Off	CH2 Vert: 2V/div.
Frequency knobs: cw	Trigger: CH2.
	Display: CH1.

Observation: The scope displays a 1.1 kHz 10 Vp-p sine wave.

3.3.3 Voltage Controlled Generator (VCG) Operation

VCG is an external electronic means of controlling the frequency of the generator by using signal levels of up to 5V peak. This allows the generator to be swept (up or down in frequency) or frequency modulated.

Control	**Setting**
Freq Range **13**	Set to the desired frequency range. Frequency can only be changed within a range.
Frequency Coarse and Fine **2**	For positive dc inputs at VCG In, set the Frequency knobs to the lower frequency limit. For negative dc inputs at the VCG In, set the Frequency knobs to the higher frequency limit. For modulation with an ac input at VCG In, set the Frequency knobs at the desired center frequency
VCG In **18**	As required.
Mode **15**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-3).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Lin/Log **10**	Select desired mode.

NOTE

Excessive VCG input voltage may cause nonlinear operation when the generator attempts to exceed the range limits.

The generator can be swept up to 1100:1 with a 5V input signal to the VCG In connector. With the frequency set to 1100, excursions between – 5 and 0V at VCG In provide a 1100:1 decreasing frequency. With the frequency set to 0001, excursions between 0V and + 5V at the VCG In provide a 1100:1 increase frequency within the frequency range.

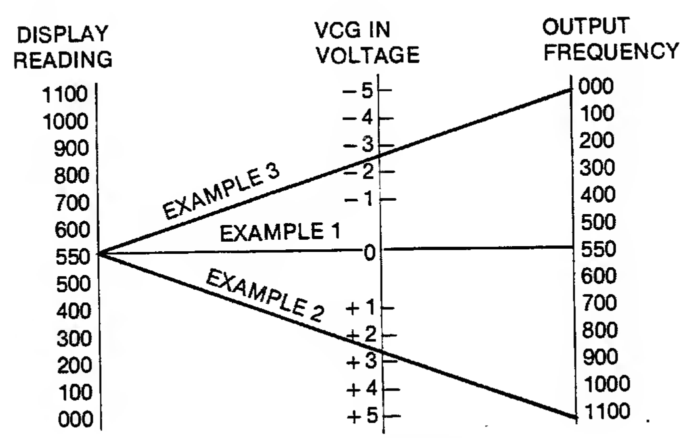
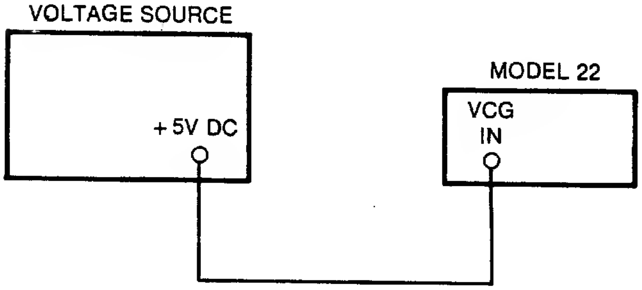


Figure 3-6. VCG Nomograph

The VCG nomograph, figure 3-6, gives examples of how an input voltage affects the output frequency (LIN). Example 1 shows that with 0V VCG input, the Frequency knobs determine the output frequency. Example 2 shows that a positive VCG input increased the output voltage. Example 3 shows that a negative VCG input decreases the output frequency. In the nomograph decimal points are not shown. The output frequency must be multiplied by the range. For example, in example number 2 if the frequency range is set to the .001 to 1.100 kHz range, the display will read .550 kHz and when the VCG voltage is applied the display will read 1.1 kHz.

To demonstrate VCG operation, connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	Voltage Source Settings
Power: On	Output level: +5Vdc.
Frequency knobs: ccw	

Observation: The display reads approximately 1.1 kHz.

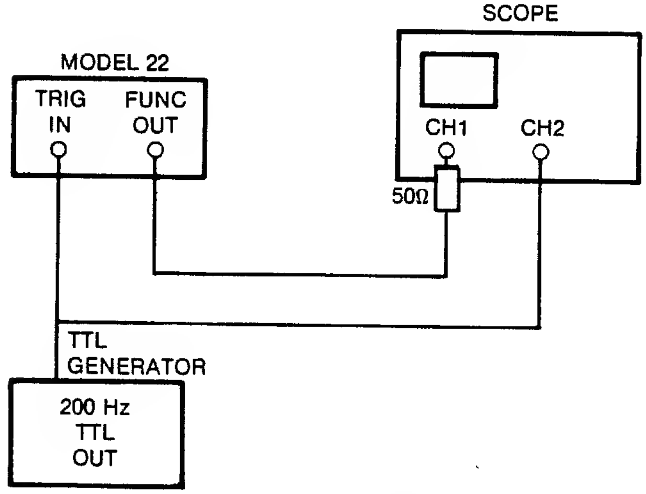
3.3.4 Triggered Operation

A triggered generator produces a single waveform each time a trigger signal is received. The Model 22 can be triggered by manual control or with a TTL signal.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (−20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Mode **15**	Select Trigger.
Trig In **16**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Trigger **8**	Press to trigger.

The triggered waveform starts from a quiescent point i.e., sine and triangle (0Vdc), square and ramp up (lower level), ramp down (upper level). All waveforms may be d.c offset). The Model 22 triggers on the rising (_/‾) edge of the trigger signal.

To demonstrate trigger operation, connect the instruments as shown below, then set the controls as listed below.



Model 22 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	CH2 Vert: 2V/div.	
D.C. Offset: Off	Trigger: CH2	
Mode: Trigger	Display: CH1 and 2.	

Observation: Scope Channel 1 displays a single 1.1 kHz, 10Vp-p sine wave coincident with the rising edge of the trigger input signal (CH2).

3.3.5 Gated Operation

A gated generator produces a continuous output waveform for the duration of the trigger signal. The Model

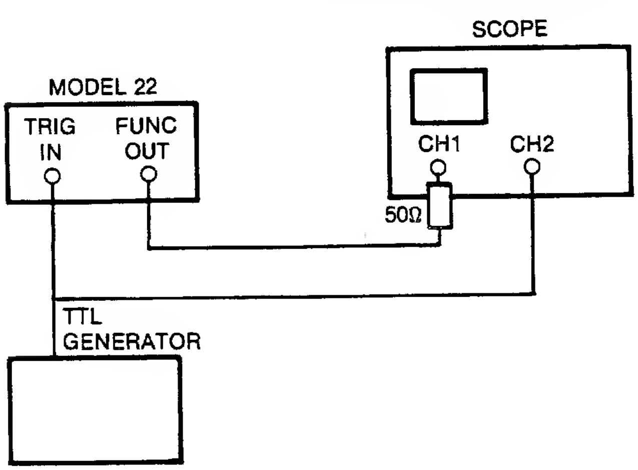
22 can be gated by manual control (Trig Switch) or with an external TTL signal (Trig In).

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (− 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (− 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **16**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Mode **15**	Select Gate.
Trigger **8**	Press in to start gate; release to stop gate.

The gated waveform starts from a quiescent point i.e., sine and triangle (0Vdc), square and ramp up (lower level), ramp down (upper level). All waveforms may be dc offset.

The instrument gates from the rising edge () to the falling edge () of the Trig In signal. The last cycle started will be completed.

To demonstrate gate operation, connect the instrument as shown below, then set the controls as listed below.



Model 22 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200 Hz.
Amplitude: cw	CH1 Vert: 2V/div.	Output
D.C. Offset: Off	CH2 Vert: 2V/div.	Level: TTL
Frequency knobs: cw	Trigger: CH2.	
Mode: Gate	Display: CH1 and 2	

Observation: Scope CH1 displays gated sine waves starting at the rising edge of the trigger input (CH2) and ending after the falling edge of the trigger input.

3.3.6 Stabilizer Operation

The stabilizer, when turned on, locks the frequency to the display frequency reading. Stabilizer circuit maintains the generator frequency at this setting. The stabilizer works on all frequency ranges. Thus, the frequency range can be changed without unlocking the stabilizer.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **15**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (− 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (− 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).
Stab **19**	Select On.

3.3.7 Sweep

The Model 22 uses an internai generator to linearly or logarithmically change the output frequency. The unit can be continuously swept or triggered swept.

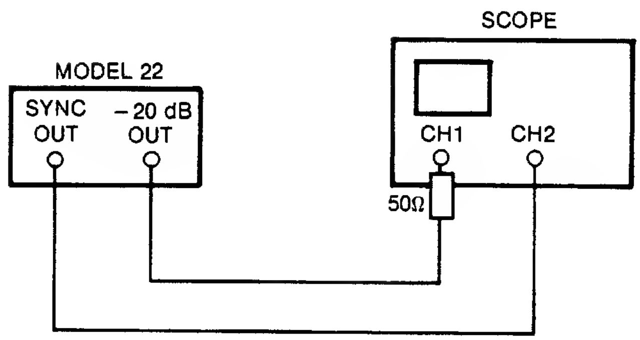
3.3.7.1 Continuous Sweep

For continuous sweep, the generator sweeps from the start frequency to the stop frequency in a continuously occurring sweep.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Mode **15**	Select continuous to set the start frequency, Set to set the stop frequency, and, finally, Sweep for continuous sweep.
Frequency Coarse and Fine **2**	These controls set the desired start frequency within a range. In the Continuous mode, the display **1** shows the start frequency.
Swp Set **5**	This control sets the desired stop frequency within a range. In the Set mode, the display **1** shows the stop frequency.
Lin/Log **10**	Select either linear or logarithmic sweep.
Swp Time **12**	Select one of the four sweep times. Sweep rate should be << generator waveform frequency.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **17**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.

Model 22 Settings	Scope Settings
Power: On	
Mode: Continuous Frequency knobs: Set to 0.001 kHz	Time base: 1ms/div. CH1 Vert: 2V/div.
Mode: Set Frequency knobs: Set to 1.100 kHz	CH2 Vert: 2V/div.
Mode: Swp	Trigger: CH2 (– slope) Trigger Mode: Norm Display: CH1 and CH2
Amplitude: cw D.C. Offset: Off Lin/Log: Lin Func: sine wave	



Observation: The Model 22 continuously sweeps from approximately 1 Hz to 1.100 kHz at a 0.01 second rate.

3.3.7.2 Triggered Sweep

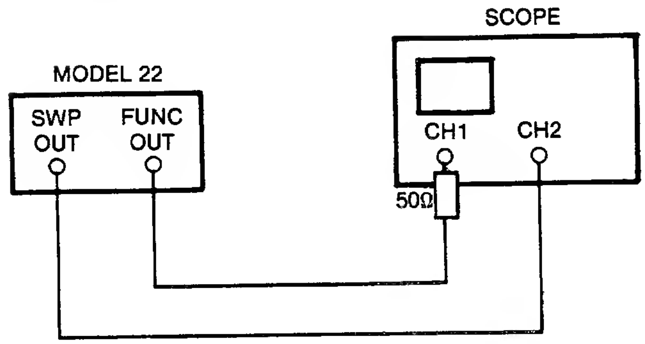
For triggered sweep, the generator sweeps from the start frequency to the stop frequency upon receipt of a trigger. The trigger can be handled in two differenct ways. First, if the trigger input returns low before the output reaches the stop frequency, the output returns to a quiescent level (same as in triggered mode). If the trigger input remains high after the output reaches the stop frequency, the output returns to the start frequency.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range. In the Continuous mode, the display **1** shows the start frequency.
Swp Set **5**	This control sets the desired stop frequency within a range. In the Set mode, the display **1** shows the stop frequency.
Lin/Log **10**	Select either linear or logarithmic sweep.
Swp Time **12**	Select one of the four sweep times.

D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Mode **15**	Select Continuous to set the start frequency, Set to set the stop frequency, and Trigger Sweep for that mode.
Trigger **8**	Press for manual trigger.
Trig In **16**	For external trigger, connect to TTL signal source.
Func **16**	Set to desired function.
Func Out (50Ω) **7** or Func Out (– 20 dB) **9**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate triggered sweep operation, connect the instruments as shown below, then set the controls.

Model 22 Settings	**Scope Settings**
Power: On	
Mode: Continuous	Time base: 10ms/div.
Frequency knobs: Set to 0.001 kHz	CH1 Vert: 2V/div.
Mode: Set	CH2 Vert: 2V/div.
Swp Set: Set to 1.100 kHz	
Mode: Trigger Sweep	Trigger: CH2
	Trigger Mode: Auto
Swp Time: 1 Sec	Display: CH1 and CH2
Amplitude: cw	
D.C. Offset: Off	
Lin/Log: Log	
Func: sine wave	
Trigger: Press once and immediately release it.	



Observation: The output is at a quiescent state until the manual trigger is pressed. At this time the output sweeps from approximately 1 Hz to 1.1 kHz in 1 second and returns to the quiescent state.

Trigger: Press and hold until completion of sweep.

Observation: The output is at a quiescent state until the manual trigger is pressed. At this time the output sweeps from approximately 1 Hz to 1.1 kHz in 1 second and returns to 1 Hz.

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The Model 22, an 11 MHz stabilized sweep function generator, operates as an analog waveform generator at frequencies above 1.100 kHz and a digital waveform synthesizer at frequencies below 1.100 kHz. The frequency, regardless of range, can be stabilized to the display frequency. In addition, all frequency ranges may be logarithmically or linearly swept.

As shown in figure 4-1, the function generator loop, controlled by Frequency Coarse and Fine verniers, VCG In, Trig In and the stabilizer (ASWP), is the heart of the generator. On the top four frequency ranges (11.00 kHz, 110.0 kHz, 1.100 MHz, and 11.00 MHz), the function generator loop produces triangle and square waves that are routed directly to the function selector located in the output block; a sine converter, also in the output block, modifies the triangle into a sine wave. The waveform synthesizer, which is clocked by the function generator loop via the stabilizer (MFSQ), produces all the waveforms on the five lower frequency ranges (110.0 mHz, 1.100 Hz, 11.00 Hz, 110.0 Hz, and 1.100 kHz). The synthesizer output, like on the top four frequency ranges, is routed through the function selector to the output. For all ranges, the output block selects and controls the output signal at the Func Out (50Ω), Func Out(– 20dB), and

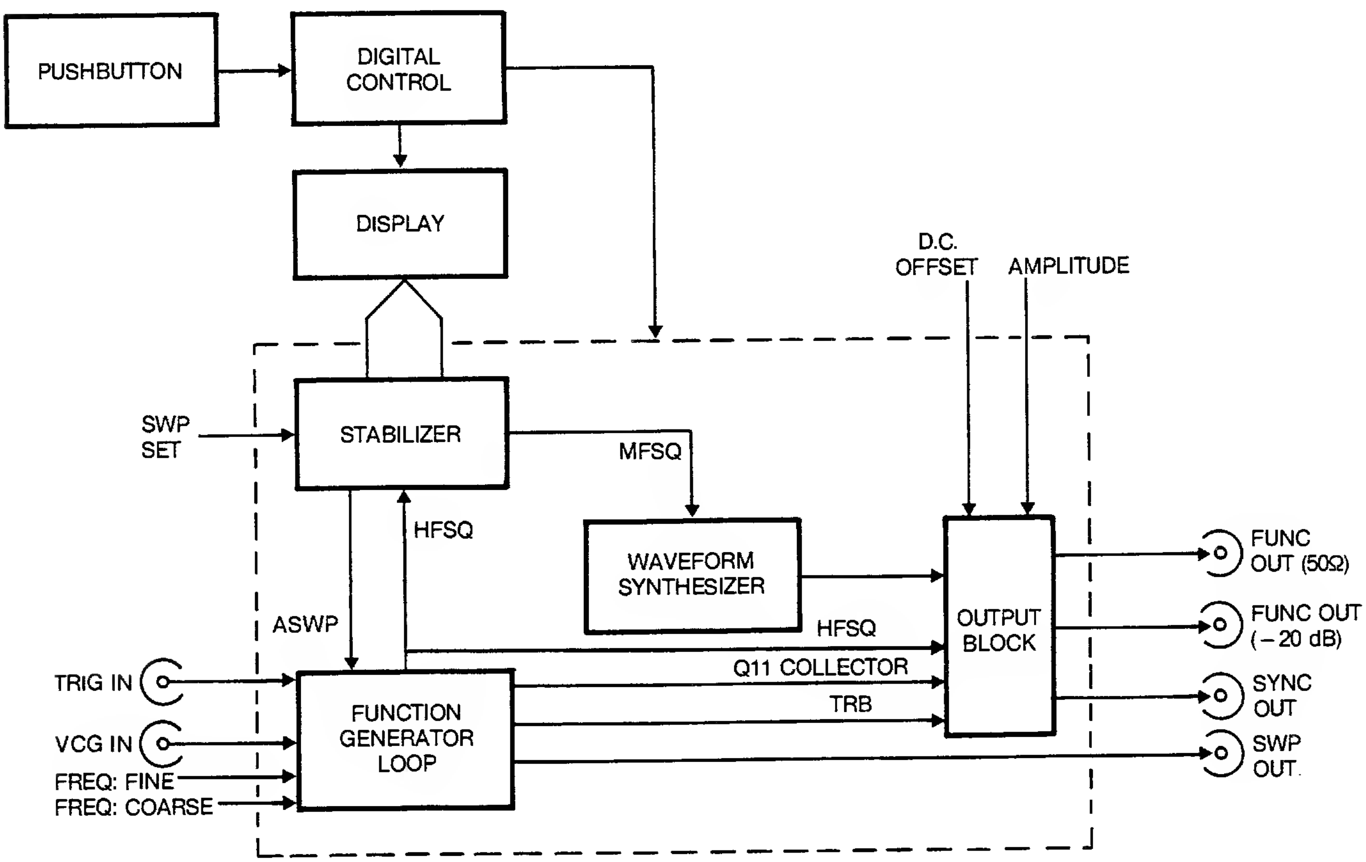


Figure 4-1. Model 22 Block Diagram

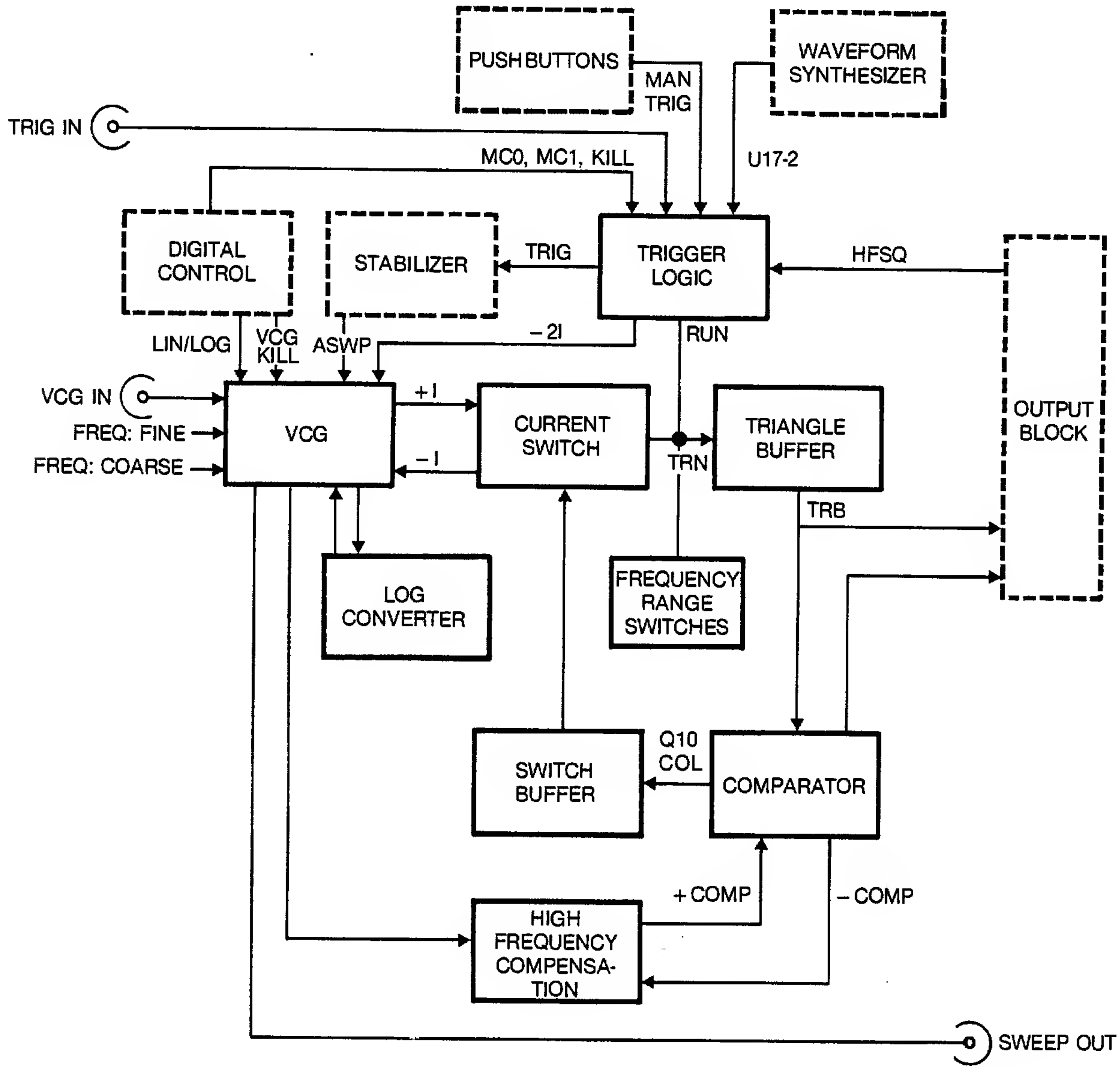


Figure 4-2. Function Generator Loop

Sync Out connectors; the output block is controlled by the digital control, Amplitude and DC Offset controls. The stabilizer, when in Stab mode, monitors the frequency, the same as shown on the display, from the function generator loop and supplies a feedback voltage (ASWP) to the function generator loop; thus the stabilizer keeps the frequency within one least significant count regardless of the frequency range. Also, the stabilizer circuit sweeps the function generator loop by increasing the voltage (ASWP) over a period of time.

The digital control sets the circuits shown in the dotted outline to a default state each time the unit is turned on. The front panel pushbuttons via the pushbutton interface causes the digital control to change parameters in the various control circuits. The digital control along with the stabilizer controls the front panel display's digits and annunciators.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Function Generator Loop

Figure 4-2 shows an expanded diagram of the function generator loop that consists of the VCG (voltage controlled generator), log converter, current switch, fre-

quency range switches, triangle buffer, comparator, switch buffer, high frequency compensation, and trigger logic circuits.

The VCG produces two currents (+I and −I), alternately switched in and out by the current switch and controlled by the output of the switch buffer, that charge (+I) or discharge (−I) one of four range capacitors in the frequency range switches to produce a linear triangle. The specific frequency is determined by the magnitude of the +I and −I currents. The triangle buffer amplifies the triangle and drives the comparator. The comparator detects the triangle peaks which causes the comparator to switch output states; the threshold level of the comparator is controlled by the high frequency compensation circuit. The output of the comparator controls the switch buffer output state which, in turn, controls the current switch. The function generator loop only produces the top four frequency ranges, the five lower ranges are produced by using the function generator loop to clock the waveform synthesizer. The log converter supplies the VCG with a current logarithmically proportional to the Frequency knobs' settings and VCG In voltage. The trigger logic circuit enables or disables the function generator loop depending on the selected mode.

4.2.1.1 VCG

The VCG (ref: schematic 0103-00-1116 sheet 1) consists of the VCG amplifier, current sources, current sink, and trigger control current sink. The VCG amplifier (U1 pin 1) converts voltages from the VCG In (except in Stab mode), FRFINE (Frequency Fine), FRCOARSE (Frequency Coarse), and ASWP (stabilizer or sweep) into currents that controls the current source and sinks (U28). The magnitude of the current sets the frequency within the selected range. A gain adjustment (R1) controls the top-of-range frequency, where as R13 sets the 1100:1 (bottom-of-range) frequency. R11 controls the offset of the amplifier and zener diode CR1 limits the voltage swing at U1 pin 1 to within 30% over the maximum allowable swing. CR2 and CR3 prevent excessive voltages at VCG In from damaging the VCG amplifier.

Current Source and Current Sink: The current source and current sink supply the current charging (+I) and discharging (−I) the frequency range capacitor. The negative signal from the VCG amplifier (U1 pin 1) is converted into a current leaving summing node at U1 pin 9 through R1 and R12. U1 pin 8 controls current sunk by Q1 which, in turn, controls current sourced by the two transistors in the upper half of U28.

Operational amplifier (U1 pin 8) holds pin 9 at ground potential. When pin 9 tries to go negative, pin 8 goes positive, which causes Q1 to sink current through R18. This lowers the voltage at the base of the two transistors in U28. Feedback resistor R204 provides a return path for the increased current through U28 pin 15 to hold U1 pin 9 at 0V. Increased current also flows from the current source (U28 pin 12). CR4 limits the voltage swing at U1 pin 8 to within 30% of the maximum allowable swing.

An increase in current through R42 pin 16 appears like a positive input to the operational amplifier (U1 pin 5) driving the output at pin 7 positive. This raises the voltage at U28 pin 1, causing pin 3 to sink more current to maintain a virtual ground at U1 pin 5. Increased current now flows into the current sink (−I) through U28 pin 6 which tracks the current source. The emitter resistors for Q4 and U28 pins 2 and 4 are all 1kΩ, therefore the collector currents at U28 pin 3, −I (pin 6), and Q4 will be equal.

Trigger Control Current Sink: The trigger control current sink clamps the triangle node (TRN) at ground potential during the "off" state in the triggered and gated modes.

When the generator is gated "off", RUN goes low reverse biasing CR7. As the triangle at TRN rises towards the zero crossing point, a greater proportion of the −2I current, emitter resistor at U28 is 500Ω, flows through U3 pin 9. Equilibrium is reached when the trigger holding current is equal to the positive current (+I) being supplied to the generator loop, preventing the triangle node voltage from rising any further. The matched diodes in U3 have equal currents through them [(−I)+(−I)=(−2I)] and the anode at pin 4 is grounded, hence the voltage drops across the two diodes are equal and the triangle node is held at ground potential. This stops the triangle waveform on the rising slope and ensures that at least one complete cycle will be generated every time the generator is triggered. Also, refer to paragraph 4.2.1.9 Trigger Logic.

4.2.1.2 Log Converter

The log converter transforms the linear change of the frequency knob to a logarithmic current that controls the current source. The logarithmic converter (ref: schematic 0103-00-1116 sheet 1) consists of transistor Q3 and amplifier U24 that uses the logarithmic base-emitter characteristics of the output half of the transistor (Q3) to produce the logarithmic current. Varying the output transistor's emitter voltage controls the current.

The converter receives its input from the VCG input circuit at R31. A constant 3mA through R34 keeps the input transistor's base-emitter voltage at −0.7V. When the Frequency knob is set at minimum frequency (0V), the emitters are biased at −0.7V (base of the output

transistor is fixed at −0.3V by R36) which places 0.4V between the output transistor's base and emitter and supplies 1μA control current to the current source.

When the frequency knob is set at maximum frequency (−7.5V), the base of the input transistor is biased at −0.3V, thus biasing the emitters at −1V. This places the output transistor's base-emitter bias at 0.7V which supplies 1mA to the current source. Thus, the linear change in base to emitter voltage of the transistor generates an exponential change in collector current.

4.2.1.3 Current Switch

The current switch (ref: schematic 0103-00-1116 sheet 2) consists of the diode switches (CR10, 11, 12, 13), current source buffer (Q7) and current sink buffer (Q17). Controlled by the square buffer, the current switch allows the charging (+I), and discharging (−I) of the selected frequency range capacitor (see Frequency Range Switches) to produce a triangle waveform.

The current switch sources current buffered by Q7 (+I) or sinks current buffered by Q17 (−I) at the switch output (junction of CR10 and CR12). The instantaneous polarity of the switch buffer output control line (junction of R59 and R60) determines the direction of current flow.

With the control line at +2V which reverse biases diodes CR11 and CR12, the +I current through CR10 charges the selected timing capacitor. At the same time, current flows from the control line through CR13 into the current sink. With the control line at -2V which reverse biases diodes CR10 and CR13, the timing capacitor discharges through CR12 to the current sink and the +I current is sourced through CR11 into the control line.

4.2.1.4 Frequency Range Switches

The frequency range switches (ref: schematic 0103-00-1116 sheet 2) consist of the four basic range capacitors and their controls. Each range capacitor or set of capacitors covers 10% to 100% of full scale. A logic level signal from the frequency range control circuit switches in the range capacitor. For example, when $\overline{FR6}$ goes low, it turns on Q22 which sources about 30 mA through R108 and diodes CR25 and CR26. With CR26 forward biased, the diodes impedance to ground is less than 2Ω and the range capacitor set (C40, C41 and C42) is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, Q22 is turned off, and R109 pulls the anode of CR25 to −15V. The voltage divider (R106, R107) biases the anode of CR26 to −7.5V reverse-biasing CR26 which provides a very high impedance to ground effectively disconnecting the range capacitor. Frequency range control lines ($\overline{FR4}$ or $\overline{FR5}$) operate the same way by connecting matched capacitors of 0.0047 μF (C43) or 0.047 μF (C45) to the triangle node (TRN) line. Capacitance for the highest frequency range (100 pF) consists of all the stray capacitance at TRN and the 11 MHz adjustment capacitor (C39 and C38). Frequency range control line ($\overline{FR6}$) connects an additional 400 pF (C41, C42) and the 1.1 MHz adjustment (C40) to TRN.

4.2.1.5 Triangle Buffer

The triangle buffer (ref: schematic 0103-00-1116 sheet 2), a high speed FET input voltage follower with a low impedance output and unity gain, buffers the current switch and frequency range capacitor from relatively high current circuits in the output block and the comparator.

The triangle buffer consists of Q14, acting as a high input impedance source follower, and Q15, acting as a low output impedance emitter follower. The difference between the input and output voltage of the circuit is controlled by adjusting the current through Q14, such that, the gate-source voltage is equal and opposite to the base-emitter drop of Q15, this causes the two voltages to cancel each other. The baseline adjustment (R103) sets the current through Q14.

4.2.1.6 Comparator

The comparator (ref: schematic 0103-00-1116 sheet 2) detects the peak of the triangle and produces two separate square wave outputs. One square wave output from the comparator (Q10 collector) drives the switch buffer, while a second square wave of opposite polarity (Q11 collector) drives the output block. The comparator's threshold voltage is set by the +COMP and −COMP from the high frequency compensation circuit.

When the triangle voltage at the base of Q19 reaches the positive threshold voltage (+1V at U3 pin 2), Q19 turns on as Q18 turns off. When Q18 and Q19 switch, they cause the second differential pair, Q10 and Q11 to switch. As Q10 switches "off", current through R63 decreases and the collector of Q10 goes low, (about −1.6V); the current drain through R90 determines the collector voltage of Q10. CR17 and CR18 increase the transistor switching speed of Q18 and Q19 by limiting the signal swing at their collectors to about 0.7V. Resistors R64 and R71 increase the switching speed of Q10 and Q11 by providing a small current which keeps them from turning completely off, and diodes CR16 and CR19 are switched on and off to further guarantee that Q10 and Q11 do not switch off.

Diode bridge (U3 pins 5, 6, 8) operate identically to the current switch. The switch buffer output (U3 pin 6) state determines the polarity of the comparator threshold voltage (U3 pin 2). The comparator threshold voltage is limited to ±1V by the voltage drop across the 332Ω

resistor (R92), the +COMP and −COMP currents supply 3mA. The high frequency compensation circuit reduces the +COMP and -COMP currents on the highest frequency range which lowers the comparator threshold voltage at the base of Q18 to compensate for switching delays (see paragraph 4.2.1.8).

Output transistors Q10 and Q11 have different values of collector and emitter resistors to match the input requirements of each buffer.

4.2.1.7 Switch Buffer

The switch buffer (ref: schematic 0103-00-1116 sheet 2) shifts the level of the comparator's square wave to provide a voltage excursion (±2.2V) capable of driving the current switch. The switch buffer is a complementary emitter follower biased on by the voltage drops across CR14 and CR15 and controlled by the comparator output at the collector of Q10. The ±2.2V square wave output controls the current switch and the polarity of the comparator threshold voltage.

4.2.1.8 High Frequency Compensation

High frequency compensation (ref: schematic 0103-00-1116 sheet 2) circuit sets the threshold voltage of the comparator. On the lower frequency ranges (110.0 mHz through 1.100 MHz), the value of the +COMP and −COMP currents set up the comparator threshold voltage at the base of Q18; each current has a fixed value of 3mA through the resistor R92. On the 1.00 to 11.00 MHz range, the threshold voltage is lowered to compensate for switching delays in the function generator loop; this maintains the triangle peaks at the same levels as on lower ranges.

On the lower frequency ranges with HF COMP disconnected, R80 and R81 holds U27 pins 2 and 3 and the emitter of Q5 at 0.0V. This puts 15V across series resistors R83 and R85 and −10V at the base of Q16. The same current that flows through R85 also flows through R52. This puts +10V at the base of Q6. The emitter of Q6 is +10.7V which causes 3mA to flow from the collector of Q6 through U3 and R92 to ground during half of the cycle setting up a threshold voltage at the base of Q18. On the opposite half of the cycle, the base of Q18 switches to −1V because the same amount of current (3mA) flows from ground through R92 and U3 to the collector of Q16.

In the 11.00 MHz frequency range, HF COMP (U2 pin 10 of the VCG) is connected to U27 pin 3. At top of the range, 2.5mA is sinked from ground through R80 and R81 to the collector of Q4 in the VCG lowering the voltage at U27 pin 3 to about −5V. This decreases the voltage at the emitter of Q5, as well as the current through R83, R85, and R52 which places the bases of Q6 and Q16 closer to their respective power supply voltages. The current through R92, the collectors of Q6 and Q16, and the threshold voltage at the base of Q18 are all decreased. This new lower threshold voltage causes the triangle to switch earlier than normal. The threshold voltage on this range is inversely proportional to the Frequency Coarse and Fine settings.

4.2.1.9 Trigger Logic

The trigger logic circuit (ref: schematic 0103-00-1116 sheet 3) allows the generator to be externally triggered or gated. When in trigger or gated modes (determined by MC0 and MC1), the Trigger Logic circuit prevents the generator from running by sinking away the current from the triangle node (TRN) that would normally charge the frequency range capacitor. Pressing the Trigger button or connecting a signal to the Trig In (TTL) BNC releases TRN to allow the generator to run until HFSQ completes one complete cycle. In addition, when the frequency range is 1.1kHz or lower, the synthesizer output (U22 pin 6) must be high to disable the function generator loop. When in DC function, $\overline{\text{KILL}}$ inhibits the generator.

The following sections describe the relationship in various conditions relative to the trigger logic.

Continuous Mode: In Continuous Mode, U12 pin 4 (MC0) is low which holds U12 pin 6 low and sets U23 pin 5 high. $\overline{\text{KILL}}$ (U22 pin 13) is high and U22 pin 11 is low for all functions except DC. This sets U23 pin 9 high enabling the function generator loop.

Trig Mode: In Trig Mode, U12 pin 4 (MC0) is held high and U15 pin 4 (MC1) is held low which forces U15 pin 6 and U12 pin 6 high. If the Trigger pushbutton is not pressed, U15 pin 10 remains high and the signal at U15 pin 8 is in phase with the Trig In signal at U21 pin 13.

With no signal present at Trig In, U23 pin 3 is low. HFSQ is low, U22 pin 8 is high, and U23 pin 5 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. U20 pin 10 (LF) is low for frequency ranges 11.00kHz and above, this forces U20 pin 8 high. Since U22 pin 2 is high, U23 pin 12 will be low. U23 pin 9 will be low disabling the function generator loop.

Each time the Trigger pushbutton is pressed U15 pin 8 goes low or on each positive transition of the Trig In signal, U23 pin 5 is clocked high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 goes low which sets U23 pin 9 (RUN) high and enables the function generator loop. At the positive transition of HFSQ (U22 pin 9), U23 pin 11 goes low. On the next negative transition of HFSQ, U23 pin 11 goes high, which clocks the low at pin 12 to pin 9 (RUN) and stops the triangle on its rising edge. Only one cycle of generator output is enabled for each trigger pulse applied.

Gate Mode: In Gate Mode, MC1 (U15 pin 4), MC0 (U12 pin 4), U15 pin 6, U12 pin 6, and U15 pin 10 are high while U23 pin 3 is low. If $\overline{KILL}$ (U22 pin 13) is high, U22 pin 11 will be high. When LF (U20 pin 10) is low (frequency ranges 11.00 kHz and above), U20 is forced high, and because $\overline{SWPRUN}$ is high in gate mode, U22 pin 3 will be low which disables the generator.

When Trigger on the front panel is pressed (U15 pin 10 goes low) or a positive transition at Trig In (U21 pin 13 goes high), U15 pin 8 goes high which clocks the Q output (U23 pin 5) high. With $\overline{KILL}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and enables the generator. As long as the trigger signal at Trig In remains high or the Trigger pushbutton is pressed, U15 pin 6 and U12 pin 6 will remain low, that sets U23 pin 5 high, forces U23 pin 10 (S) low, sets RUN (U23 pin 9) high, and enables the function generator loop by releasing TRN.

When U23 pin 3 goes low, U15 pin 6 and U12 pin 6 go high. The next negative transition of HFSQ shifts U22 pin 8 high, clocks the low at pin 12 to the output at pin 9 (RUN), and disables the triangle at 0V.

Low Frequency: When the Frequency range is 1.1 kHz or lower, the trigger logic works much the same as previously described, except U23 pin 12 must be low to stop the generator. This occurs at either the zero crossing of the rising edge of the triangle (Haver Off), or at the negative peak of the triangle (Haver On). If Haver is Off, U13 pin 6 (waveform synthesizer) functions as a zero crossing detector that controls the trigger logic. If Haver is on, U16 pin 6 (waveform synthesizer) acts as a negative peak detector. U22 pin 6 goes low in either condition. With U22 pin 6 high, the next positive transition at U17 pin 3 forces $\overline{Q}$ (U17 pin 6) low. For the five lowest frequency ranges, LF (U20 pin 10) is high, this makes pin 8 high and causes U22 pin 3 to go low.

Sweep Mode: For the three sweep modes, the trigger logic functions much the same as for the other modes. For Set and Sweep modes, the trigger logic functions exactly the same as the continuous mode. For triggered sweep mode, the trigger logic allows the function generator loop to run depending upon the condition of the Trig In signal. If $\overline{SWPRUN}$ is low, the trigger logic's RUN line remains high this allows the generator to keep running. But if $\overline{SWPRUN}$ goes high the RUN line will go low at the next positive transition at U23 pin 11, this shuts off the function generator loop and always completes the last cycle.

DC Function: If Func is set to DC, U22 pin 13 ($\overline{KILL}$) will be low. This clears U23 which forces U23 pin 9 low and disables the generator.

4.2.2 Waveform Synthesizer

The waveform synthesizer produces the digitally synthesized waveforms used on the five lower frequency ranges (1.100 kHz and below). It consists of seven circuits: ÷1/÷100 counter, reference selector, ÷1000 up/down counter, waveform EPROM, data selector, latch, and DAC, as shown in figure 4-3 and schematic 0103-00-1116 sheet 3.

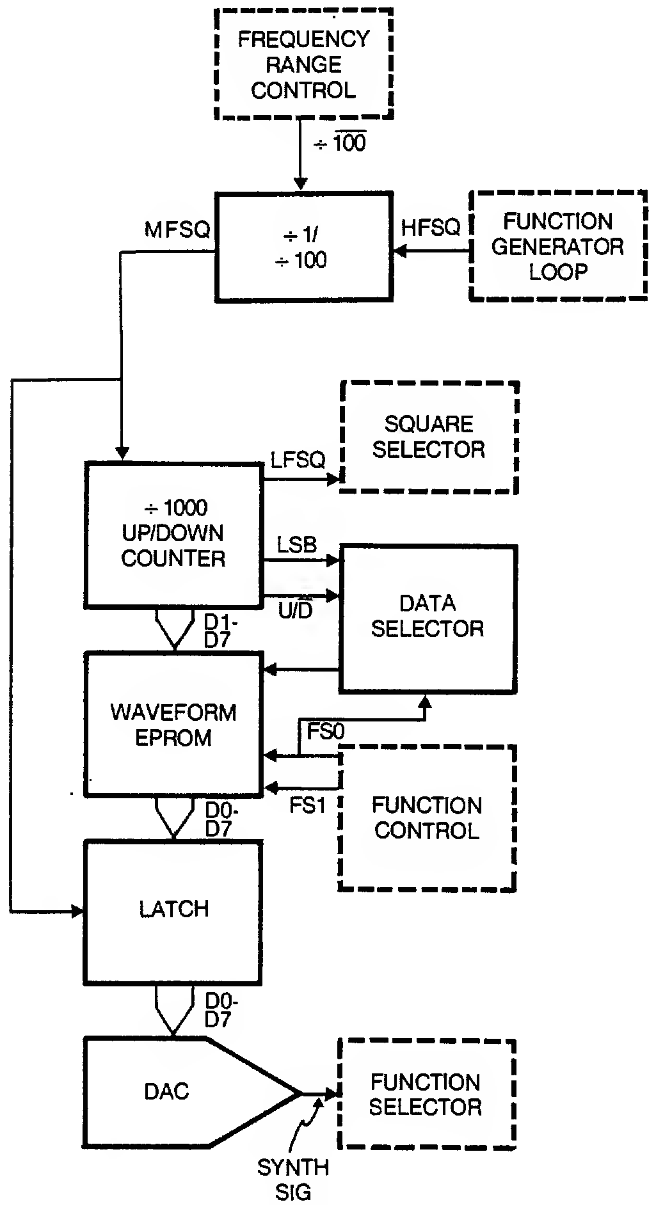


Figure 4-3. Waveform Synthesizer

The synthesizer reference originates at the function generator loop (HFSQ). This signal must pass through the ÷1/÷100 divider (U7B, U8B; ref: schematic

0103-00-1115 sheet 3) where the frequency is either divided by 1 or 100, depending upon the selected frequency range, see table 4-1.

Table 4-1. Reference Selection

Frequency Range	Generator Loop Frequency (HFSQ)	÷1/÷100	Medium Frequency Square Wave (MFSQ)
.100 to 1.100 kHz	.100 to 1.100 MHz	÷1	1.100 to 1.100 MHz
10.0 to 110.0 kHz	10.0 to 110.0 kHz	÷1	10.0 to 110.0 kHz
1.00 to 11.00 kHz	1.00 to 11.00 kHz	÷1	1.00 to 11.00 kHz
.100 to 1.100 Hz	10.0 to 110.0 kHz	÷100	.100 to 1.100 kHz
10.0 to 110.0 mHz	10.0 to 11.00 kHz	÷100	10.0 to 110.0 Hz

The 9-bit up/down counter (U6, U10, U11, and U14) counts from 0 to 499, then reverses and counts from 499 to 0. The counter steering circuit (U11, U16, and U18) watches for the top and bottom counts, then reverses the direction of the counter. When the counter increments, U17 pin 12 is low and pin 8 is high. At the top count, U18 pin 1 toggles high disabling the counter for one cycle. Also at the top count, U17 pin 12 goes high and on the next clock pulse from U15 pin 11, U17 pin 8 (the counter up/down control line) goes low, causing the counter to begin to decrement, returning U18 pin 1 to its original low state. At the bottom count, U18 pin 1 again goes high and disables the counter for one cycle. U17 pin 12 goes low, and on the next clock pulse from U15 pin 11, U17 pin 8 goes high, this causes the counter to begin to increment. U18 pin 1 again returns low.

The counter output drives the inputs of EPROM (U9) which contains the data needed to produce the sine, triangle, ramp up, and ramp down waveforms. The status of lines FS0 and FS1 determine the waveform by selecting which block of data as accessed; see table 4-2. For sine and triangle waves, the EPROM produces one half cycle, negative to positive peak, on the up count (0 to 499), then uses the same data in reverse, positive to negative peak, on the down count (499 to 0). The data from the EPROM (U9) is latched through U8 to DAC U7.

Table 4-2. EPROM Control Lines

FS0	FS1	Function
0	0	DC
0	0	Sine wave
0	1	Triangle
1	0	Ramp up
1	1	Ramp down

The DAC converts the data from the EPROM into a current, SYNTH SIG, for the function selector.

The synthesizer can also produce ramp up and ramp down waveforms. These ramps are stored in the EPROM (U9), as are the sine and triangle waveforms. To produce the ramps, the line FS0 goes high; the line FS1 selects either the ramp up (FS1: low) or ramp down (FS1: high). In generating the ramps, the up/down counter functions the same as it does for triangles and sine waves; counting 0 to 499 and 499 to 0, except that the least significant bit to the EPROM is controlled by the data selector (U11, U12). The U/D line (U17 pin 9) is the complement of the line, it causes the counter to count up or down. When counting up, U/D is low which holds the least significant bit low. This allows only even addresses to be accessed. When counting down, U/D is high, the least significant bit is held high and only odd addresses are accessed.

4.2.3 Stabilizer

The stabilizer serves three functions. First, it measures the generator's frequency and drives the frequency display. Second, it compares the displayed frequency, stored in latches, against the actual frequency of the generator and makes slight frequency corrections to the generator's frequency. And third, it steps the function generator loop through the sweep range. Figure 4-4 shows a block diagram of the stabilizer block.

4.2.3.1 Timing Generation

This circuit provides the timing control for the stabilizer. As shown in schematic 0103-00-1115 sheet 2, the 6.4 MHz oscillator consists of crystal (Y1) and differential amplifier (U9A). The output of this oscillator is divided to 50 kHz by U8A (at pin 9).

Four divide-by-10 counters (U5A, U6A) together with their control devices, produce the GATE, MEMCLK, FRCHG, and CLRCNT pulses which control the frequency comparator circuit. Figure 4-5 shows the timing diagram for the counters.

4.2.3.2 Prescalar

The prescalar (ref: schematic 0103-00-1115 sheet 3) selects the clock for the 3½ digit BCD counter. The clock frequency, regardless of the selected range, will always be between 1.00 and 11.00 kHz. The prescalar block consists of the HFSQ divider and selector.

The HFSQ divider (U9C, U8C) divides the HFSQ square wave from the generator loop by 10, 100, and 1000. Each of these outputs drive the selector circuit. In addition, the divider includes the ÷1/÷100 counter (U7B) for the synthesizer block.

The selector (U9B), controlled by the frequency range control, determines which HFSQ divider output will drive

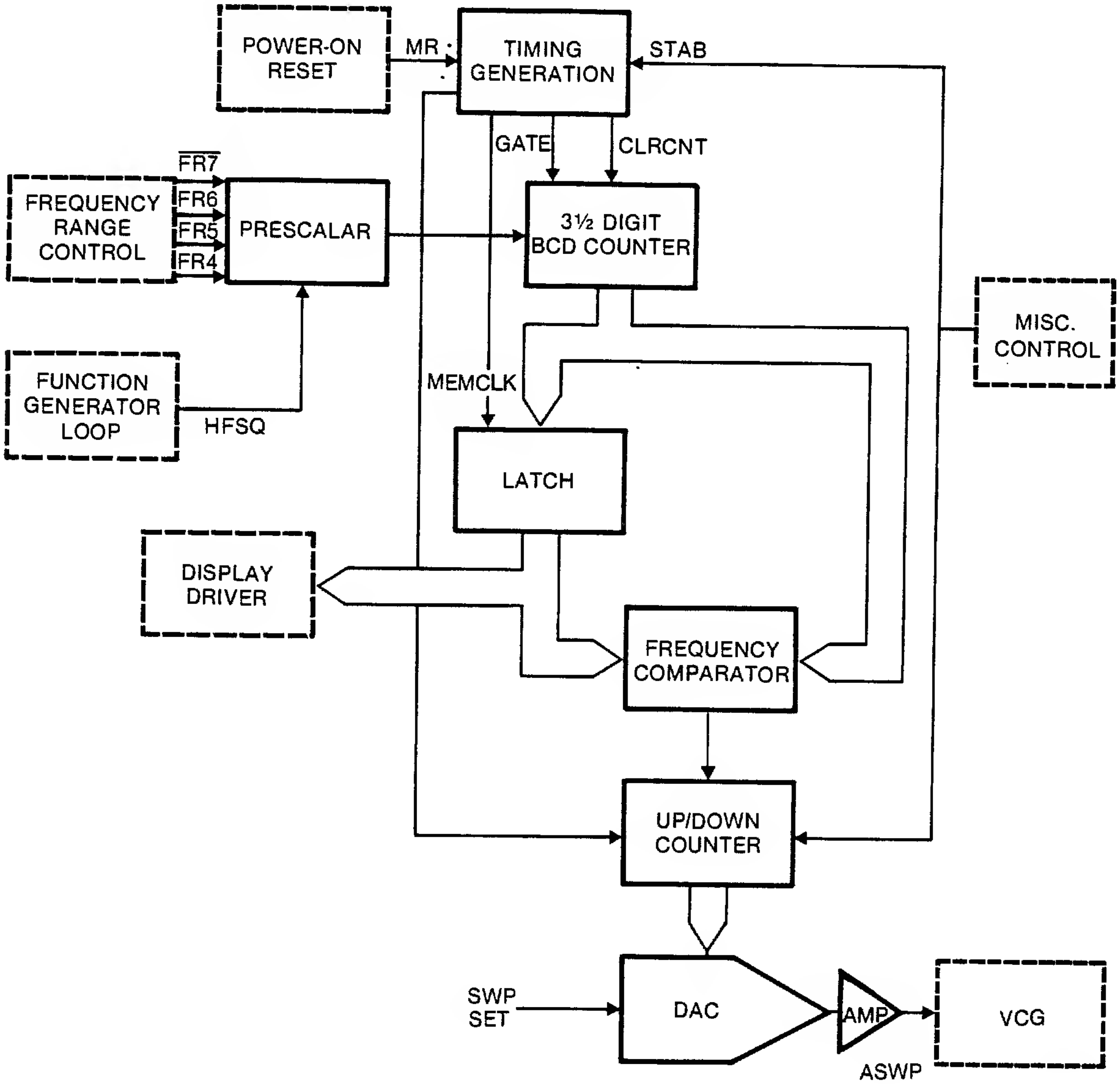


Figure 4-4. Stabilizer

the BCD counter. Table 4-3 shows the relationship between the ranges, generator loop frequency, and division ratio.

4.2.3.3 Frequency Counter

The frequency counter (ref: schematic 0103-00-1115 sheet 3) consists of a control flip flop (U6F) and four cascaded BCD ripple counters (U1A, U2A). This counter tallies the number of cycles from the prescalar over a 100 ms period. The output lines from the counter drive the frequency comparator.

When the GATE line goes high, the control flip flop (U6F) is enabled to allow the counter to count until the GATE

Table 4-3. Prescalar

Selected Freq Range (Hz)	Actual Function Generator Loop (Hz) Frequency	Divider	Counter Clock (Hz)
1.00 – 11.00 M	1 – 11 M (FR7)	÷ 1000	1 – 11 k
.100 – 1.100 M	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0 k	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00 k	1 – 11 k (FR4)	÷ 1	1 – 11 k
.100 – 1.100 k	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00	1 – 11 k (FR6)	÷ 100	1 – 11 k
.100 – 1.100	10 – 110 k (FR5)	÷ 10	1 – 11 k
10.0 – 110.0 m	1 – 11 k (FR4)	÷ 1	1 – 11 k

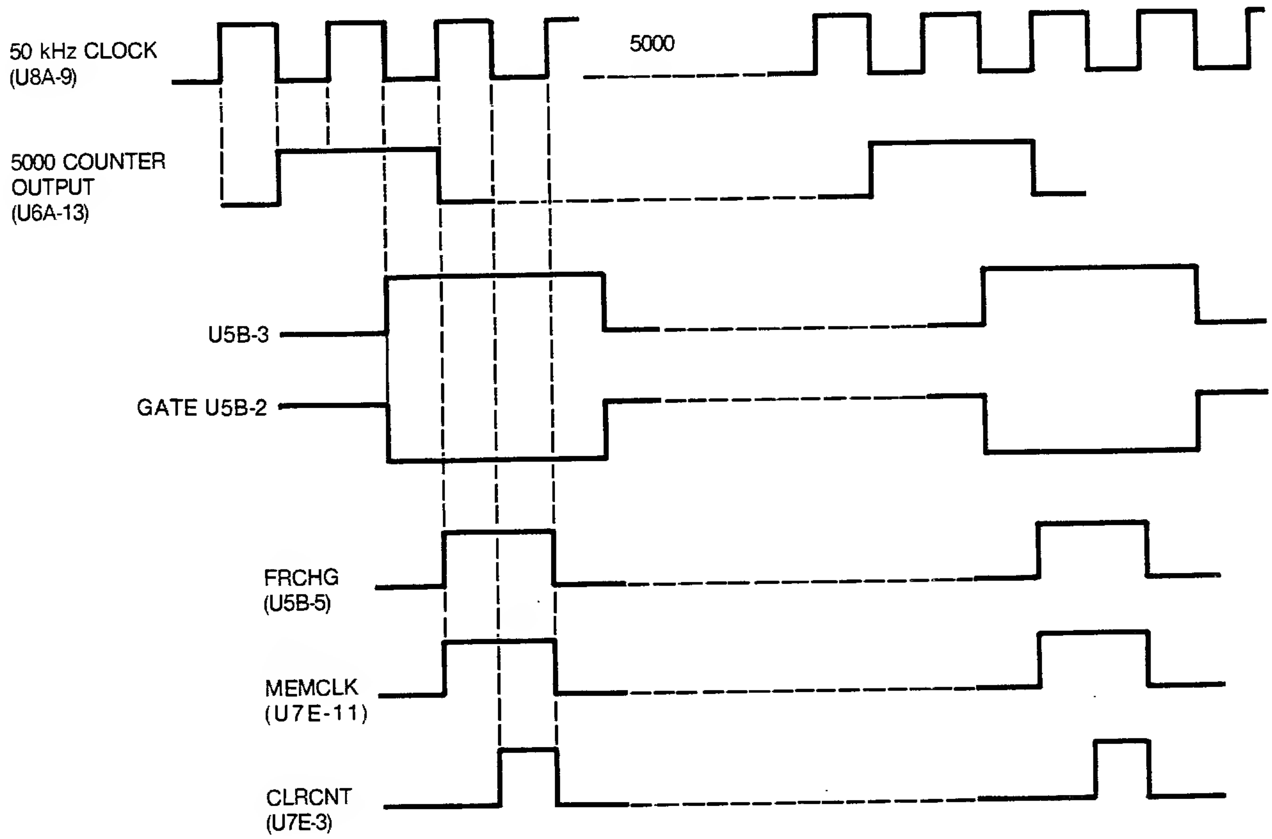


Figure 4-5. Timing Generation

line goes low, which inhibits the control flip flop. Approximately 20 μs after the GATE line inhibits the flip flop, the CLRCNT line clears the flip flop and counter, and when the GATE line returns high, the frequency counter again counts the frequency. For GATE and CLRCNT timing relationships, see figure 4-5.

4.2.3.4 Frequency Comparator

The frequency comparator (ref: schematic 0103-00-1115 sheet 3) serves two functions. First, it is part of the frequency display. Second, stabilizer enabled, it compares the input from the frequency counter with the stored frequency shown on the display. The resulting output at the two latches (U1B, U3B) and two comparators (U2B, U4B) controls the frequency correction or sweep block.

Latches: The latch (U1B, U3B) receives its data directly from the frequency counter. The MEMCLK, when it goes high for 20 μs, clocks the frequency data to the output registers of the latches. Outputs from the latch drive both the display drivers and Q inputs of the frequency comparators (U2B, U4B). The MEMCLK occurs about every 100 ms, see figure 4-5 for timing relationships.

When the stabilizer is enabled, the MEMCLK line remains low holding the frequency data (displayed frequency) stored in the latches.

Frequency Comparator: The frequency comparator consists of two individual comparators (U2B, U4B) that are daisy chained together via gate U6C. It monitors data from the frequency counter and compares the data (P and Q) with the outputs from the latches. This produces two control lines that control the up/down counter in the frequency correction or sweep circuit.

When the stabilizer is off, the P and Q lines are always the same (P = Q). When the stabilizer is on, the P data can change while the Q data remains unchanged. The comparator detects the change and switches its two output lines (U4B pins 1 and 19) as shown in table 4-4. In sweep modes, Q6 is forced high and P6 is held low which forces the comparator output to P<Q; this causes the frequency correction and sweep circuit to always count up.

Table 4-4. **Comparator — U/D Counter Relationship**

Condition	U4B Pin 19	U4B Pin 1	Correction U/D Counter
P = Q[1]	Low	High	Counter Disabled
P<Q[2]	High	High	Counts Up
P>Q	High	Low	Counts Down

NOTE

P Frequency data from the frequency counter.
Q Frequency data from the latches.
1 Also Stabilizer off condition.
2 Also Sweep condition.

4.2.3.5 Frequency Correction or Sweep.

When the stabilizer is on, the frequency correction circuit (ref: schematic 0103-00-1115 sheet 3), controlled by the frequency comparator, makes frequency corrections to the function generator loop. For sweep modes, the correction block steps the generator's frequency from a start frequency up to the stop frequency. This block consists of the 8-bit up/down counter (U9F, U8F) and the DAC (U8G) along with its summing amplifier (U9G).

8-Bit Up/Down Counter: The 8-bit up/down counter (U9F, U8F), controlled by two lines from the frequency comparator, uses its output to increment or decrement the DAC. Table 4-4 illustrates how the comparator controls the up/down counter. The counter preloads (1000 0000) for stabilizer to the center of the counter's range; for sweep modes it load to the bottom of the counter's range. If the stabilizer is on, the FRCHG pulse clocks the counter every 100 ms; see figure 4-5. In sweep modes FRCHG rate varies depending on the sweep time. When the stabilizer is turned on, the STAB line from the misc control logic goes high to enable the counter. For stabilizer off, the STAB line goes low and on the next FRCHG clock transition the outputs all go to a TTL low, except the most significant bit which is held high. The eight data lines from the counter directly drive the inputs of the frequency correction DAC.

Digital to Analog Converter and Summing Amplifier: The digital to analog converter (U8G), DAC, converts the 8 bits of digital data from the 8 bit up/down counter into a proportional analog current. The amplifier (U9G) sums the DAC's current to produce a voltage that, when the stabilizer is on, drives the ASWP input of the function generator loop. The reference voltage for the DAC depends upon the mode of operation. For the stabilizer mode, the reference is set by resistor R29 to the +15V supply. For sweep modes, the reference is set by the Sweep Set control (SWDTH).

4.2.3.6 Trigger Sweep Logic

The trigger sweep logic (ref: Schematic 0103-00-1115 sheet 3) detects the two kinds of sweep trigger that will control the function generator loop. If TRIG remains high at the end of the sweep, the generator returns to and runs at the start frequency. If TRIG returns low before the end of the sweep, the generator returns to its quiescent state (0Vdc).

The following describes the operating cycles for the trigger sweep logic circuit. The TRIG input goes high which clocks flip-flop (U9E pin 5) high thus resetting flip-flops U9D pin 4, U9D pin 10, and U9E pin 10. With U9D's $\overline{Q}$ output low ($\overline{SWPRUN}$), the function generator loop starts operating. Also, U9D pin 9 is preset high forcing U9E pin 7 low which enables the up/down counter.

If TRIG remains high at the end of the sweep time, then SWPRUN remains low but the counter will overflow (U8F pin 15 goes low) which holds the up/down counters. But when TRIG goes low before the end of the sweep, flip-flop U9D pin 6 ($\overline{SWPRUN}$) goes high which shuts off the generator. Also, the up/down counter overflows (U8F pin 15 goes low) which holds the up/down counters.

4.2.4 Output Block

The output block, shown in figure 4-6, consists of the square buffer, square selector, square shaper, sine converter, function select, preamplifier, output amplifier, and attenuator. It also has output protection circuits for both Func Out BNCs. The output block selects the appropriate waveform and connects it to the Func Out BNCs.

4.2.4.1 Square Buffer

The square buffer (ref: schematic 0103-00-1116 sheet 2) amplifies the square wave from the function generator loop (Q11 collector). The output (HFSQ) drives the trigger logic, frequency counter, and square selector. The square buffer is similar to the switch buffer (ref: paragraph 4.2.1.7) except for output phasing and output level: 0 to +5V. A highly differentiated portion of HFSQ is coupled through C24, C25 and C31 to the triangle node (TRN) to counteract switching transients coupled through the current switch.

4.2.4.2 Square Selector

The square selector (ref: schematic 0103-00-1116 sheet 3) picks either HFSQ from the square buffer or the low frequency square wave from the synthesizer. Outputs from the square selector drive the square shaper and Sync Out connector.

Above the 1.1 kHz frequency range, LF (U20 pin 13) is low which enables U20 pin 4 and routes HFSQ to the

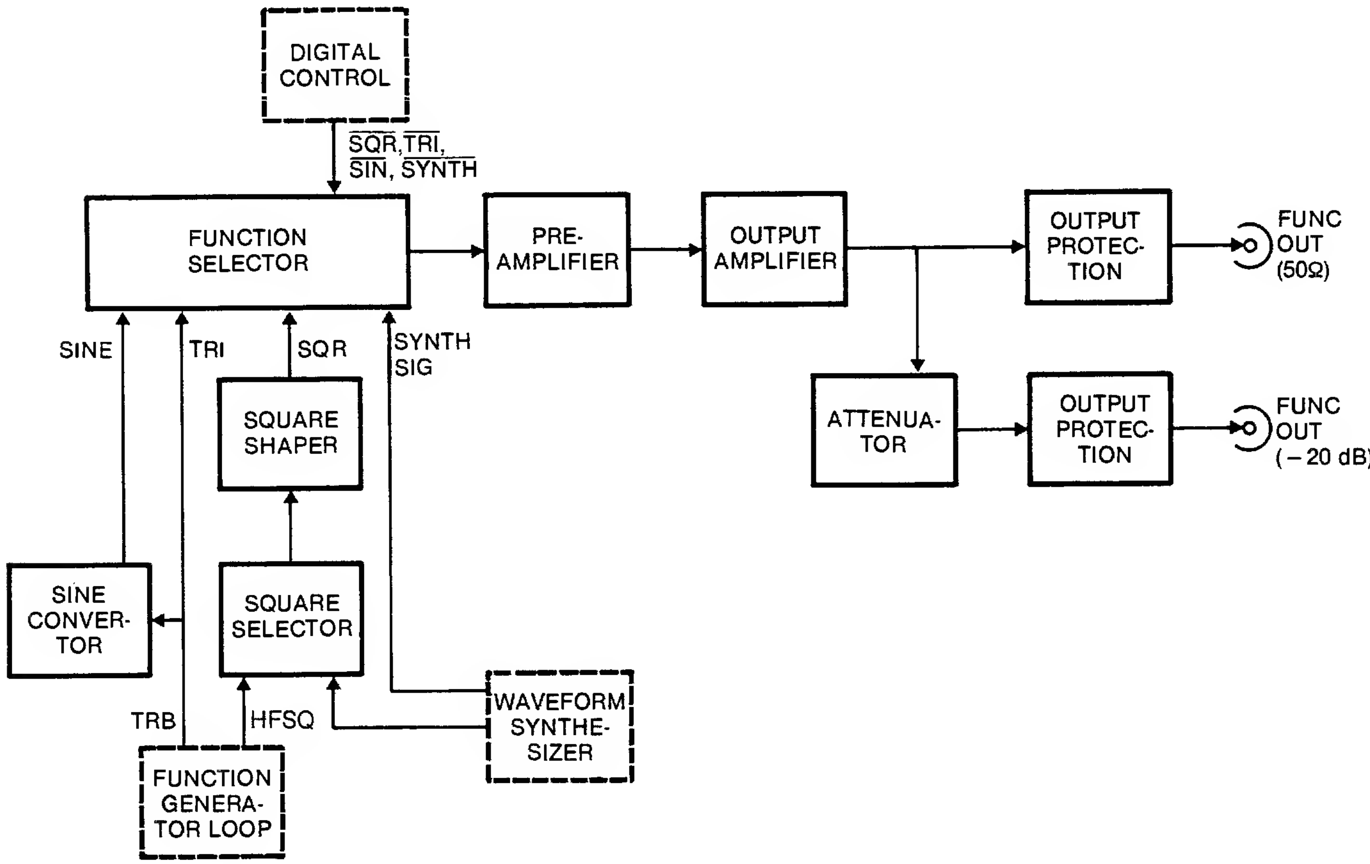


Figure 4-6. Output Block

Sync Out (U21 pin 6) and TTL SQ (U16 pin 12). For frequency ranges 1.1 kHz and below LF (U19 pin 9) is high, this enables U20 pin 3 and routes the square wave from the waveform synthesizer to the Sync Out (U21 pin 6) and TTL SQ (U16 pin 12).

If Func is set to square wave, $\overline{SQR}$ at U19 pin 5 will be low, which puts U16 pin 1 high. The signal at U16 pin 2 will pass in phase to the square shaper via TTL SQ. For all functions other than square wave, $\overline{SQR}$ will be high disabling TTL SQ (U16 pin 12).

4.2.4.3 Square Shaper

The square shaper (ref: schematic 0103-00-1116 sheet 3) takes the TTL square wave (TTL SQ) from the square selector and converts it to a clean, fast square wave current (± 1mA) that drives the preamplifier. The square wave is created by alternately sourcing and sinking current through the diode switch (CR36 through 39).

The voltage divider (R141, CR33, CR34, CR35, R144) converts TTL SQR to a bipolar signal that switches the diodes in the square shaper. When TTL SQ is high, the voltage at the cathode of CR36 is approximately + 1.5V; CR38 sinks current from the TTL SQ signal while CR37 sources 1mA from the + 15V supply through U5 pin 6 to the preamplifier. When TTL SQ toggles low, the voltage at the cathode of CR36 is approximately − 1.5V; CR36 sources current to the TTL SQ signal and CR39 sinks 1mA from the preamplifier through U5 pin 6 to the − 15V supply. The current source and sink for upper and lower levels of square waves are independently adjustable by R142 and R147. Resistor R146 sets high frequency square wave peaking.

4.2.4.4 Sine Converter

The sine converter (ref: schematic 0103-00-1116 sheet 3) transforms the triangle into a sine wave. The sine converter uses the logarithmic response characteristics of the six matched diodes (U4) to approximate a sine wave current output. Buffered triangle signal (TRB) enters the converter at U4 pins 2, 3, and 9. SIN DIST A trim pot (R121) adjusts the converter input for diode forward

voltage variation. Two other adjustments, SIN DIST B (R132) and SIN DIST C (R137), balance the positive and negative peaks respectively. The current output is switched through FET switch (U5) when $\overline{\text{SIN}}$ is low. Tri Level trim pot (R126) adjusts the triangle waveform current that enters FET switch (U5) which is enabled by a low at $\overline{\text{TRI}}$.

4.2.4.5 Function Select

The function select circuit (ref: schematic 0103-00-1116 sheet 3) connects either the synthesizer output signal (SYNTH SIG), the square wave (TTL SQ), the sine converter output, or the buffered triangle (TRB) to the input of the preamplifier. Signal switching is handled by four section CMOS analog switch (U5). For example, when $\overline{\text{SYNTH}}$ goes low, U5 pins 14 and 15 short together which connects SYNTH SIG to the preamplifier. C57 and C58 eliminate ringing (switch bounce) on the control line. Except for signal names and component numbers, the remaining three sections are identical.

Both the triangle and sine FET switches (U5), when not selected, are isolated by shorting their inputs to ground through Q27 or Q28. For example, when $\overline{\text{TRI}}$ is high (not selected), Q26 is turned off, the collector of Q26 goes low, and Q27 is forward biased which effectively shorts the emitter of Q27 to ground.

4.2.4.6 Preamplifier

The preamplifier (ref: schematic 0103-00-1116 sheet 4) inverts and amplifies the signal current from the function selector to a sufficient voltage level for the output amplifier. The gain of the preamplifier is controlled by R184, which sets the sine wave amplitude; zener diodes CR44 and CR45 bias the preamplifier at ±9.4V.

4.2.4.7 Output Amplifier

The output amplifier (ref: schematic 0103-00-1116 sheet 4) provides the final gain and output drive of the instrument. It consists of an inverted summing amplifier (with a gain of about 10) for high-frequency signals and a differential amplifier for dc and low-frequency signals. The differential amplifier also allows the dc offset of the Func Out waveforms.

AC Signal Path: High-frequency signals couple into the symmetrical emitter followers Q29 and Q32 through capacitors C91 and C92 respectively. These emitter followers drive the symmetrical inverter stage consisting of Q30 and Q33. Diodes CR46 and CR47, along with the 10Ω resistor R175, increase the switching speed of the output stage transistors Q31 and Q34 by biasing them partially on. The output signal (±20V, maximum) feeds back through resistors R176 and R177 to the input. Two 100Ω resistors (R196 and R197) set the output impedance for the Func Out (50Ω) connector.

DC Signal Path: The dc and low-frequency path in the output amplifier is through the differential amplifier transistor array (U26). The output signal (U26 pin 3), inverted relative to the input (U26 pin 5), controls the current through transistor Q30. The signal at the collector of Q30 changes until the fed back signal through R176 and R177 balances with the input signals. The PNP transistors (U26) balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C85 limits the speed of this section at high frequencies.

Offset Circuit: When the D.C. Offset switch is turned on, the voltage on the wiper of R3 is converted to current through R167 and R168. This current is proportional to the voltage and polarity at the wiper of R3 and provides dc control of the input current and, therefore, the output voltage offset.

4.2.4.8 Attenuator

The attenuator (ref: schematic 0103-00-1116 sheet 4), two 498Ω resistors (R198 and R199) and a 54.9Ω resistor (R200), provides 20dB of attenuation at 50Ω output impedance to the Func Out (−20dB) connector.

4.2.4.9 Output Protection

The output protection circuits (ref: schematic 0103-00-1116 sheet 4) guard the output amplifier from excessive external voltages that could be accidentally connected to either of the Func Out BNCs that could damage the instrument.

There are two safeguards to protect the output amplifier.

1. Two in-line fast-blow fuses for each Func Out connector.
2. Four voltage-limiting, high current diodes (CR50 through CR53) that provide additional protection at the Func Out (50Ω) connector.

4.2.5 Pushbutton Interface

When a front panel pushbutton is pressed, an input to the pushbutton interface (ref: figure 4-7 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) is connected to either +5V or ground which switches the logic level of the pushbutton interface output. The MAN TRIG line from the pushbutton interface goes to the trigger logic, while the remaining lines go to the digital control block. Each switch drives a Schmitt trigger gate. RC circuits prevent multiple pulsing at the input of each gate. Outputs drive the appropriate control circuit within the unit.

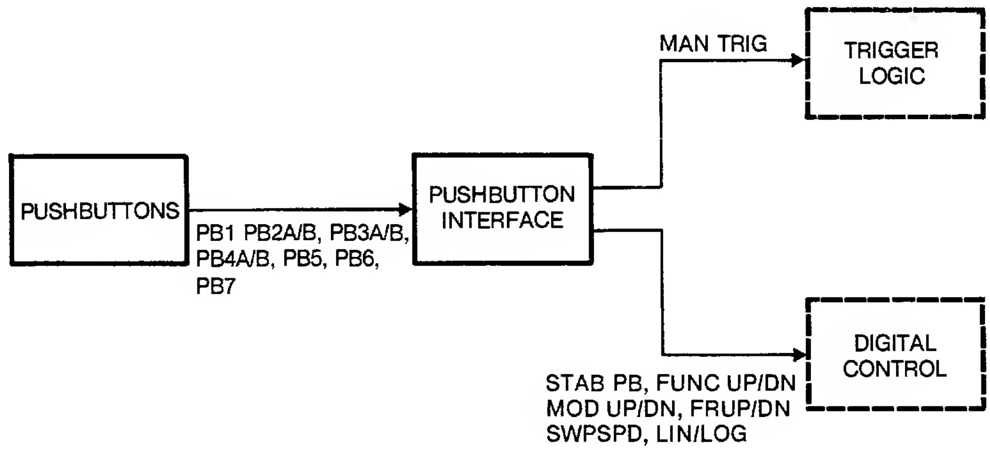


Figure 4-7. Pushbutton Interface

4.2.6 Digital Control

The digital control block (figure 4-8) consists of the power on reset, mode control, misc. control, frequency range control, function control and sweep speed control circuits.

4.2.6.1 Power-On Reset

The power-on reset circuit (ref: schematic 0103-00-1115 sheet 3) sets all other digital control circuits to a predetermined state. On initial power up, C57 holds U3G pin 13 low which causes MR (pin 12) to go high and $\overline{MR}$ (pin 4)

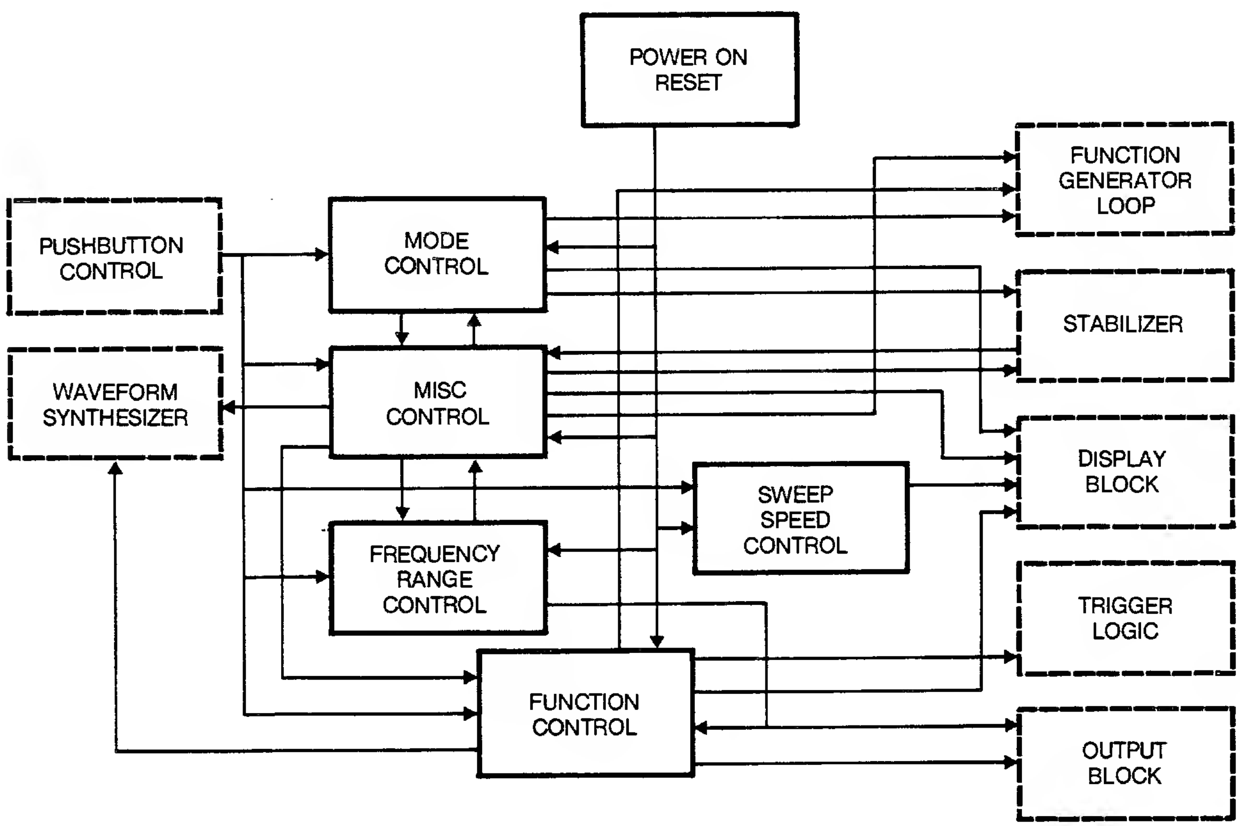


Figure 4-8. Digital Control

to go low. MR and $\overline{MR}$ reset the various digital control circuits. After about ½ second, C57 has charged to approximately 2.5V which causes MR (pin 12) to toggle low and $\overline{MR}$ (pin 4) to toggle high. These levels now remain constant for the remainder of the time the unit is on.

4.2.6.2 Mode Control

As the Mode pushbutton control lines (ref: figure 4-9) are pulsed, the mode control circuit steps through a sequence of modes either up (MODUP) or down (MODDN) from the last selected mode. This switches one of the output mode lines low. These mode lines, in conjunction with additional logic gates, control the trigger logic, stabilizer, display, and misc control; $\overline{CONT}$ combines with $\overline{STOP}$ to produce BL.

The mode control circuit (ref: schematic 0103-00-1115 sheet 2) contains the up/down counter (U4G) with separate count up (MODUP) and count down (MODDN) inputs. The counter's output drives decoder U4F that enables one of the seven modes.

The two NAND gates (U5G) limit up or down counts between gate and sweep. At one extreme (gate mode), U5G pin 8 is low, which causes pin 11 to remain high and

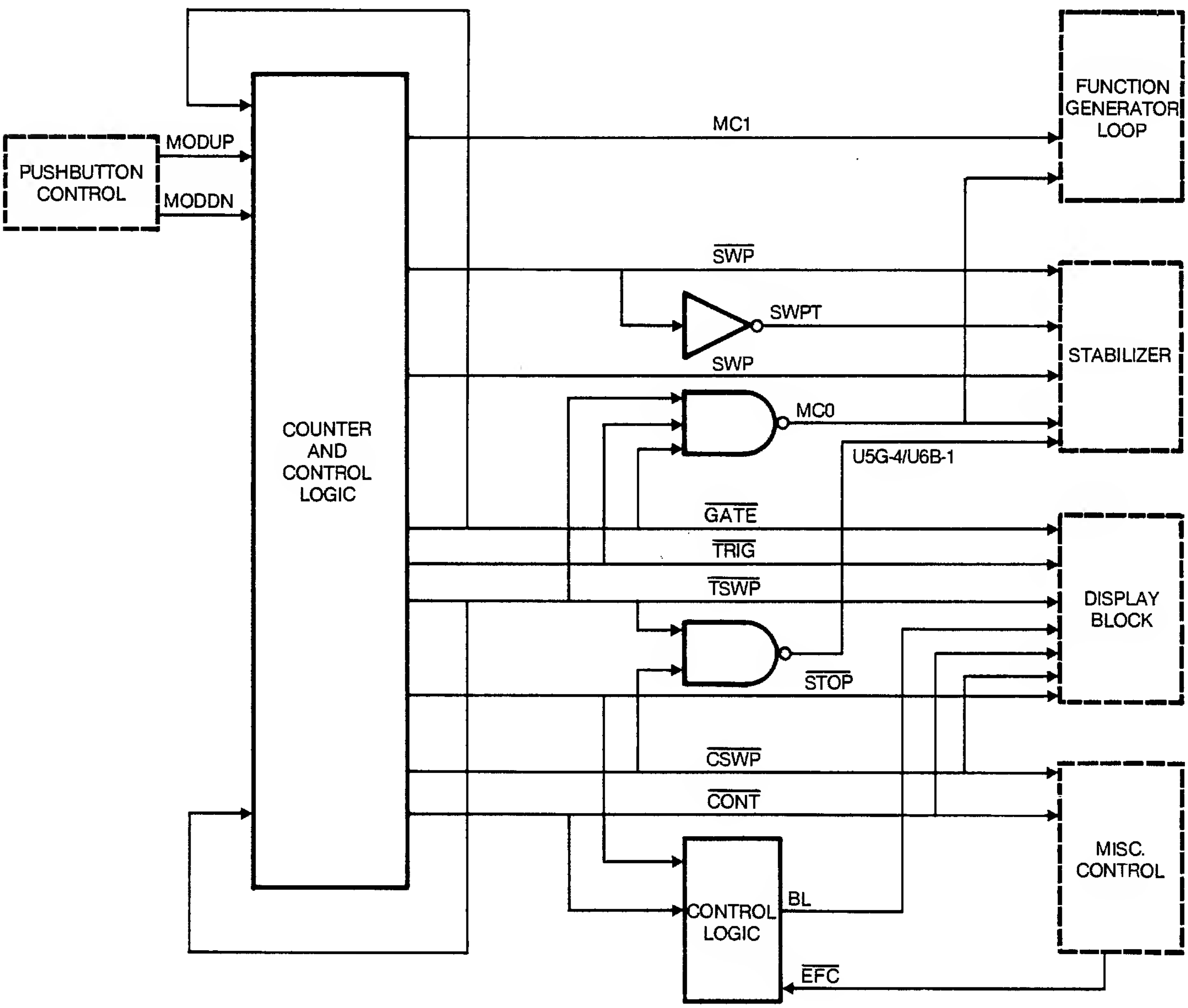


Figure 4-9. Mode Control

inhibits inputs at pin 12. In the other case (triggered sweep mode), U5G pin 8 inhibits pin 9. MC0 and MC1 control the trigger logic. $\overline{\text{CONT}}$ controls the misc. control. $\overline{\text{GATE}}$, $\overline{\text{TRIG}}$, and $\overline{\text{CONT}}$ enable the appropriate segment on the display. In trig or gate modes, BL disables all number segments of the display.

4.2.6.3 Misc Control

The misc control circuit (ref: figure 4-10 and schematic 0103-00-1115 sheet 2) receives control lines (LIN/LOG, STABPB, and EFCPB/SWPSPD) from the pushbutton interface, $\overline{\text{CONT}}$, $\overline{\text{CSWP}}$ and $\overline{\text{TSWP}}$ from the mode control, LF from the frequency frange control, and UNSTAB from the stabilizer circuit. It drives the display, stabilizer, function generator loop, frequency range control, mode control, function control, waveform synthesizer, and log converter.

Sweep Speed: The sweep speed counter (U3A) receives a pulse (EFCPB/SWPPD) from the pushbutton interface (U3G pin 10) each time the Swp Time pushbutton is pressed. This steps the counter (U3A) through four binary states which supply control lines SPD0 and SPD1. These two lines are further decoded by U4C whose outputs, through the display drivers, control the display.

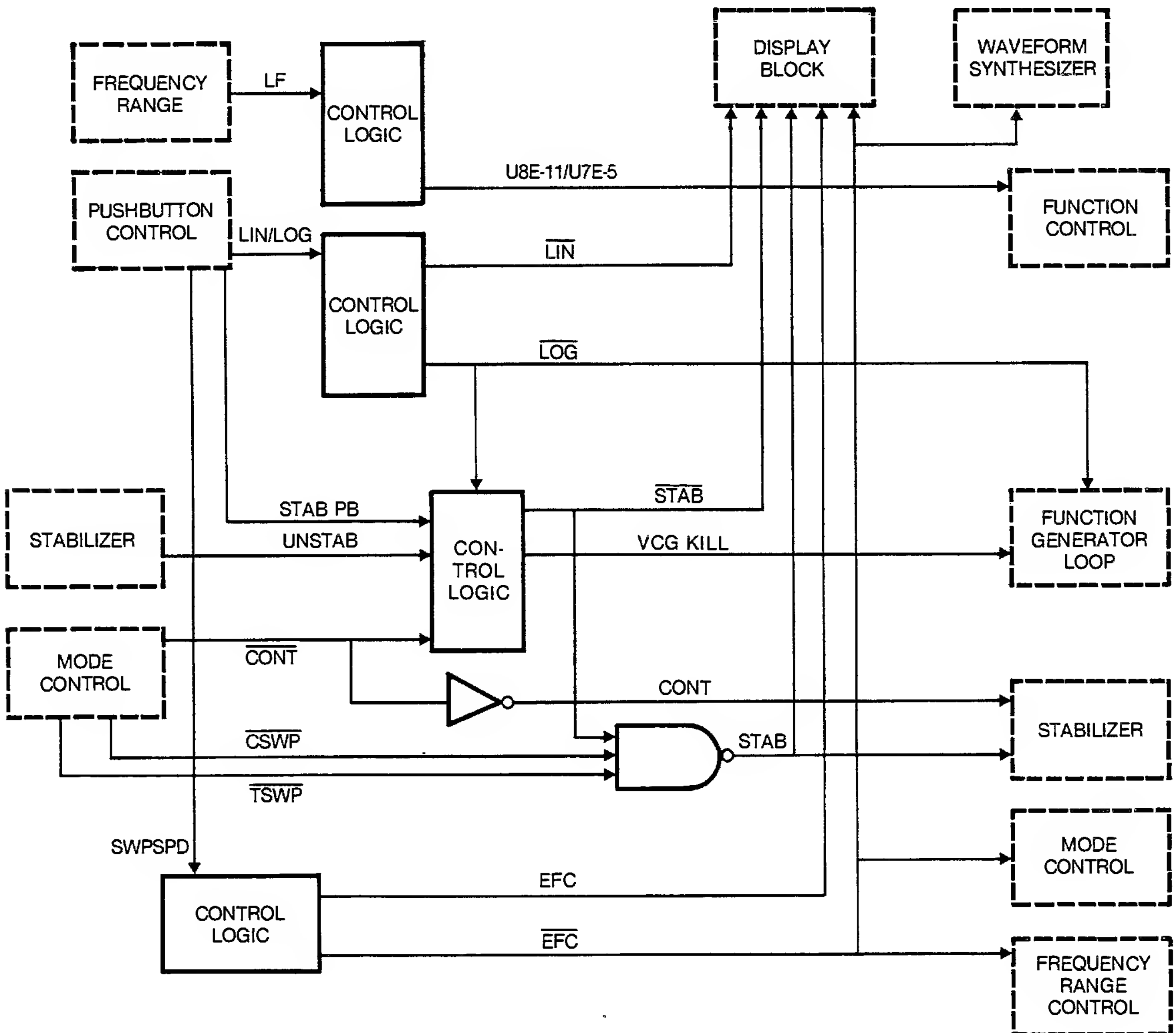


Figure 4-10. Misc Control

Lin/Log: The Lin/Log counter (U7A) receives a pulse from the pushbutton interface (U3G pin 6) each time the Lin/Log pushbutton is pressed. This causes the counter output (U7A pin 3) to change states. When $\overline{\text{LIN}}$ goes low, linear frequency change is selected.

Stabilizer: The stab flip-flop (U6F) receives a pulse (STABPB) from the pushbutton interface (U3G pin 2). Since both J/K inputs to U6F (pins 10 and 11) are always high, the two flip-flop outputs (pins 14 and 15) change state each time the flip-flop receives a STABPB pulse. When the stabilizer is off, $\overline{\text{STAB}}$ is high. U4E inverts $\overline{\text{STAB}}$ to produce STAB which, when low, allows MEMCLK to be pulsed with each transition of U7E pin 13. When the stabilizer is on, $\overline{\text{STAB}}$ is low, making STAB high, which in turn holds MEMCLK low at all times. With $\overline{\text{STAB}}$ low, VCG KILL is high which disconnects the VCG In BNC from the input of the VCG circuit. The stabilizer is disabled by U6G pin 1 if UNSTAB (U6G pin 3) goes low, the frequency exceeds the range, or a mode other than continuous is selected.

4.2.6.4 Frequency Range Control

The frequency range control circuit (ref: figure 4-11 and schematic 0103-00-1115 sheet 2) steps through a sequence of frequency ranges. As the Freq Range pushbutton is pressed, the pushbutton interface detects whether the frequency range should increase (FRUP) or decrease (FRDN). The circuit's output lines control the

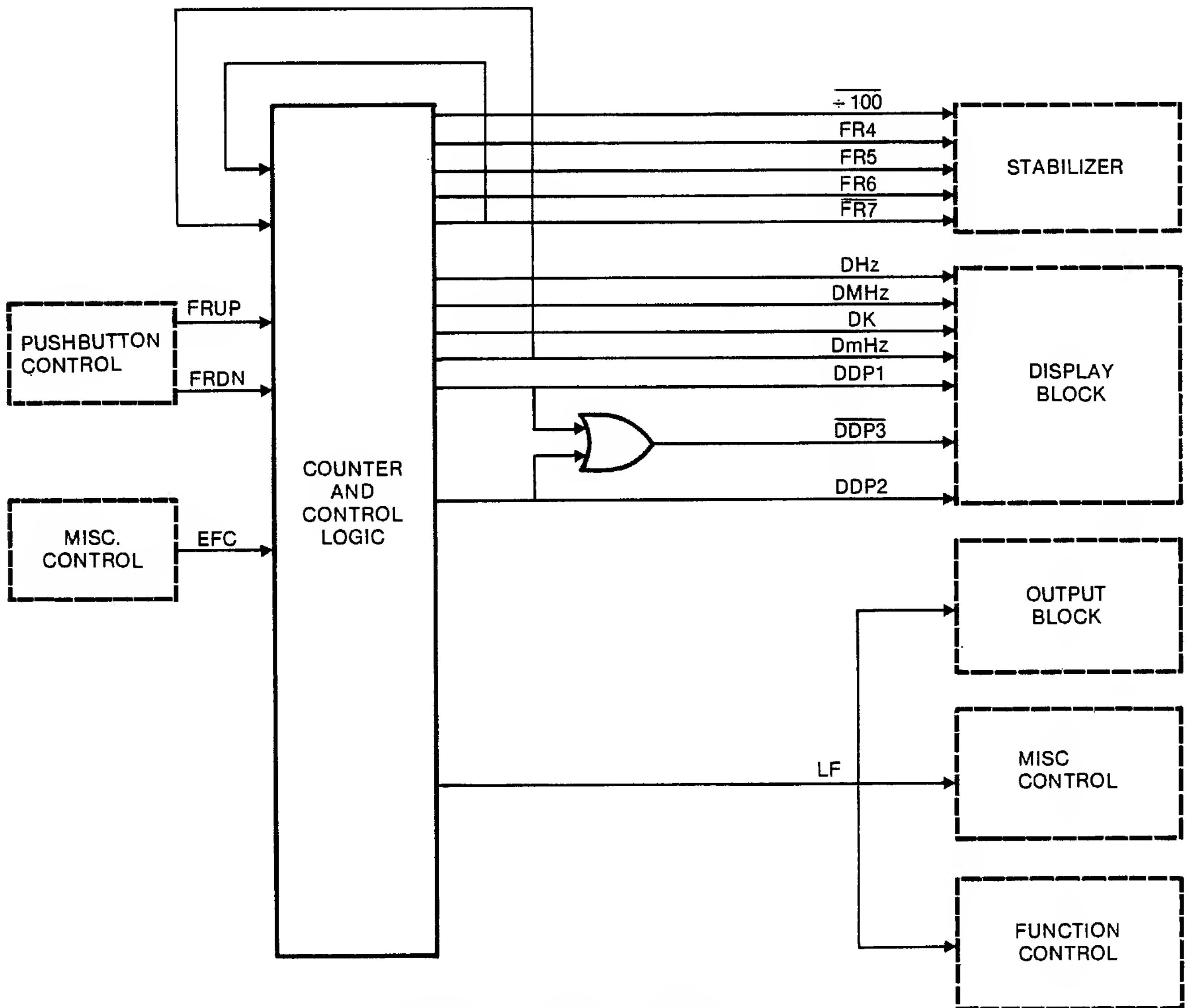


Figure 4-11. Frequency Range Control

stabilizer, display block, output block, function control, and misc control. External frequency control (EFC) combines with other control lines to produce LF.

Up/down counter (U6E), which has separate "count up" and "count down" inputs, receives pulsed signals from U5F originating from the freq range (FRUP and FRDN) pushbutton buffers. The output of this counter drives decoder (U6D), which selects one of its output lines to be low. $\overline{\text{FR7}}$, which controls the HF COMP on the analog board and goes to the frequency counter, is driven directly by one of these lines. From the remaining output lines are decoded the appropriate frequency range control lines (FR4, FR5, and FR6), which are inverted by the frequency counter circuit before going to the analog portion of the generator. The nine output frequency ranges of the generator originate from these four control lines (FR4, FR5, FR6, and $\overline{\text{FR7}}$), the low frequency synthesizer, and the $\overline{\div 100}$ control line. In the five lowest ranges, LF is high which, unless square function is selected, enables SYNTH (through the function control). This connects the output of the LF waveform synthesizer to the input of the preamplifier. The output frequency of the synthesizer is 1/1000th of the range selected. For example, if FR5 (110kHz range) is selected, the output frequency range of the synthesizer (and therefore the Func Out connectors), would be 110Hz. In addition, in the 3 lowest ranges, $\overline{\div 100}$ is low, further dividing this signal by 100. Using the same example, the synthesizer output frequency range would now be 110 mHz. Two NAND gates (U5F), serve to prevent any up or down count beyond the capability of the unit. At one extreme (110mHz frequency range), U5F pin 1 is low which causes pin 3 to remain high at all times and disables pin 2. In the other extreme, (11.00 MHz), U5F pins 8, 9, and 10 perform this function.

On the display, DmHz controls the "mHz" emblem, DHz controls "Hz", DK controls "K", and DMHz controls "MHz". The decimal points are controlled by DDP1, DDP2, and $\overline{\text{DDP3}}$.

4.2.6.5 Function Control

The function control (ref: figure 4-12 and schematic 0103-00-1115 sheet 2), which selects the instruments six functions (waveforms), consists of the input gates (U5F), up down counter (U5D), decoder (U4D), and control gates (U4E, U5E, U6E).

When the Func pushbutton is pressed, a pulse occurs on either the FUNCUP or FUNCDN lines. These lines, routed through the input gates, step the up/down counter either up or down from the last selected function. The BCD output from the counter is decoded by U4D; a low on the decoder's output represents an enabled line. The control gates (U4E, U5E, and U6C) further decode the circuits output lines. These lines control the display block, output block, trigger logic and waveform synthesizer.

The two NAND gates (U5F) prevent any up or down count beyond the limits. For dc function, U5F pin 13 is low, which disables FUNCDN at U5F pin 12. For negative going ramp, U5F pin 5 goes low which disables FUNCUP at U5F pin 6. Output lines $\overline{\text{TRI}}$, $\overline{\text{SIN}}$, and $\overline{\text{SQR}}$ in the non-synthesized frequency ranges select the waveform sent to the preamplifier. When LF (from the frequency range control) is high and the unit is in sine, triangle, or either ramp function, $\overline{\text{SYNTH}}$ is selected (low) connecting the output of the waveform synthesizer to the input of the preamplifier. FS0 and FS1 select the waveform at the waveform synthesizer output. When the unit is in square function, $\overline{\text{SQR}}$ is selected (low), connecting the output of the square shaper to the input of the preamplifier. , , , , enable the appropriate segment on the front panel display.

4.2.7 Display

The display block (ref: figure 4-13 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) consists of the display drivers and the display. Two 30 Hz signals, BP and its complement $\overline{\text{BP}}$ originating from U5C, synchronize the LCD and the segment drivers. To enable a segment of the display, 5Vrms is needed between BP and the segment control line.

The display drivers are exclusive-or gates which drive the display's bars, arrows, and decimal points and all function the same. For example, when the unit is in continuous mode, U3F pin 9 ($\overline{\text{CONT}}$) is low. The $\overline{\text{BP}}$ signal at pin 8 is in phase with the signal at pin 10 (Z3) and out of phase with BP. This results in a 5Vrms voltage of between BP and Z3, which enables the segment. When the unit is not in Cont mode, a high at pin 9 causes the output at pin 10 to be in phase with BP which results in 0Vrms and disables the segment. Data for these gates originate from the various digital control circuits in the unit.

Lines D2A through D4D, which originate from the frequency comparator, determine which number segments are enabled. Each output line (2A through 4G) drives a number segment except in Trig or Gate modes when they are disabled by BL.

4.2.8 Power Supply

Three power supply voltages, +15V, −15V, and +5V are generated on the power supply circuit board (ref: schematic 0103-00-1113).

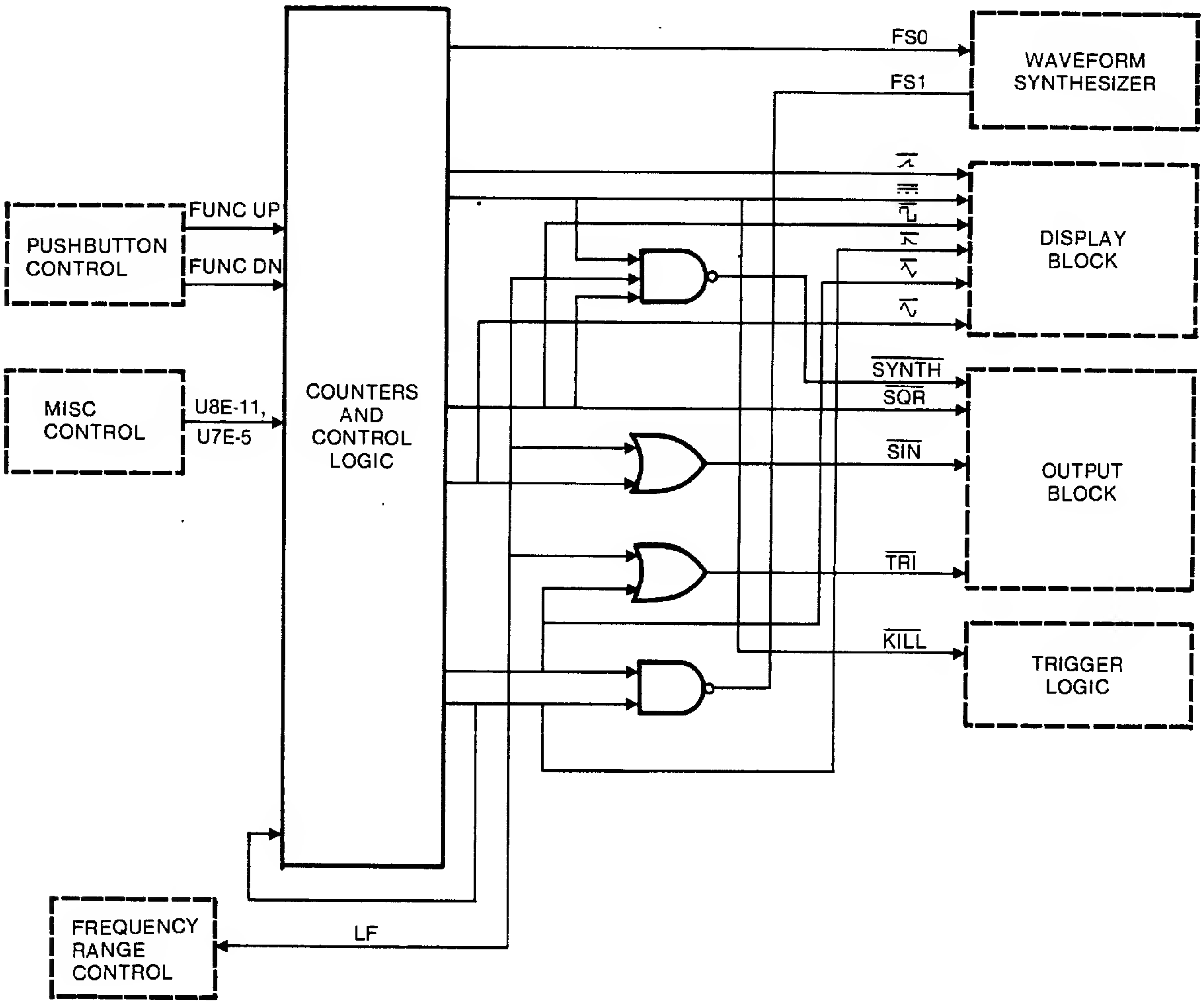


Figure 4-12. Function Control

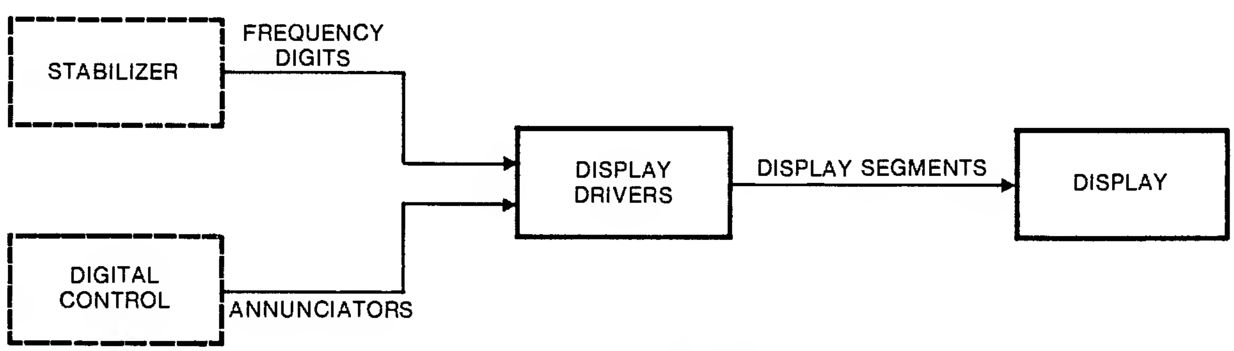


Figure 4-13. Display Block

4.2.8.1 +5V Supply

In the +5V supply, ac from the transformer T1 (located on the rear panel), is rectified by CR2 and filtered by C9, C10, and C11 to provide unregulated dc for regulator VR2. This three-terminal regulator normally operates with a 1.25V difference between its input and output terminals. C12 provides additional filtering at the output of the regulator.

4.2.8.2 ±15V Power Supplies

The ±15V Power Supplies provide power to the analog sections of the instrument. R2, which is in series with the output of the +15V regulator, causes current limiting to take place at a lower value than the internal limiting provided by the regulator. As the current through R2 reaches its limiting value, the voltage drop across R2 reaches 0.4V. Any further current through R2 causes the regulator to lower the output voltage until the current falls back to the limiting value.

The −15V supply operates similarly to the +15V supply, however the polarities are reversed.

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter	Millivolt dc measurement (0.1% accuracy), true rms
Oscilloscope, Dual Channel	≥100 MHz bandwidth
Counter	20 MHz (0.01% accuracy)
50Ω Feedthru	±0.5% accuracy, 2W
Distortion Analyzer	To 200 kHz
RG58U Coax Cable	3 ft length BNC male contacts
Spectrum Analyzer	To 60 MHz
Pulse Generator	40 Hz, 5 to 15 ms pulse width, TTL level.

5.3 CALIBRATION

NOTE

Before removing the cover, disconnect the instrument from the ac power source. Refer to Section 2 for cover removal, except leave top cover on and remove only bottom cover for calibration. Invert the instrument so generator board adjustments are on top and place the bottom cover on top of the unit to maintain the operating temperature during calibration.

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. Figure 5-1 shows waveform generator board calibration points.

> *NOTE*
>
> *The completion of the calibration procedure returns the instrument to correct alignment.*
>
> ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS***
>
> *Instrument specifications are given in Section 1 of this manual.*

1. All measurements made at the FUNC OUT connector must be terminated into a 50Ω (±0.5%) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing the bottom cover, connecting the unit to an ac source, and setting these front panel switches as follows:

Frequency	
Fine	cw
Coarse	cw
Amplitude	cw
D.C. Offset	Off
Swp Set	cw

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Lift bottom cover only to make adjustments or measurements.

Table 5-1. Calibration Procedure

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
1	Power Supply Regulators	dc Voltmeter	J10 Pin 2	Paragraph 5.3 step 2			Black (−) lead ground
2			J10 Pin 5			−15V ± 350 mV	Red (+) lead dc volts
3			J10 Pin 6			+5V ± 250 mV	
4			J10 Pin 7			+15V ± 350 mV	
5	Triangle Amplifier Balance		J10 Pin 3		R103	0V ± 100 mV	Rough adjustment only
6					R86	0V ± 20 mV	
7	Function Out	Scope	Func Out (50Ω)			10Vp-p sine wave (Approximately 2 cycles)	Terminate with 50Ω Scope Settings: 2V/div. 0.2 ms/div.
8				Step Func button to right		Functions match display (correct amplitude and frequency)	
9	Output Amplifier Balance			Func: ⎓ (dc)	R157	0V ± 10 mV	Display shows 00.0 kHz Scope setting: 10 mV/div. (or maximum scope sensitivity if more than 10 mV)
10	Trigger Baseline			Func: ∧∨ Frequency knobs: fully cw Freq Range: 110.0 kHz Mode: Trig	R103	0Vdc ± 50 mV	Scope setting: 0.1V/div. Verify baseline 0VDC ±100 mV over full range of Coarse Frequency knob (Frequency Fine knob full cw)
11	VCG Zero	DC Voltmeter	VCG In BNC	MODE: Cont Func: ⊓⊔ Frequency knobs: fully ccw	R11	0V ± 0.5 mV	Use coax cable with no termination.
12	1100:1 Frequency	Scope	Func Out (50Ω)		R13	First transition occurs at center vertical grid line, for 50 Hz.	Use coax cable with 50Ω termination. Scope settings: 2V/div. 2ms/div. Trigger slope: − (Neg) Horizontal position: Trace begins at extreme left vertical grid line
13	1100:1 Symmetry				R38	Second transition occurs at extreme right vertical grid (within 2% (1 minor division)	Repeat steps 12 and 13 if necessary. Alternate method: magnify X10 and alternate trigger slope between + and −, set R38 for <2 divisions assymetry.
14	Low Log			Lin/Log: Log	R36	One cycle >6 divisions	Scope setting: 2ms/div. 2V/div. R19 may be trimmed ⩾1 MΩ to obtain the correct result

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
15	High Symmetry	Scope	Func Out (50Ω)	Lin/Log: Lin Frequency knobs: fully cw Freq Range: 11.00 kHz	R20	<0.1% (½ minor div.) symmetry	Scope setting: 2V/div. 10 μs/div. X10 Magnification. Alternate trigger slopes while adjusting R20 for minimum assymetry.
16				Coarse Frequency: 5kHz	Verify only	<0.5% asymmetry (Verify 2½ minor divisions)	Scope setting: 20 μs/div. Magnification: Off
17	Sine Distortion	Distortion Analyzer		Frequency knobs: fully cw Func: ∿	R121, R132, R137, R86	Minimum distortion (typically 0.2 to 0.3%)	Adjust R86 slightly if necessary.
18	Full Scale Frequency	Counter		Func: ⊓⊔	R1	11.15 kHz on display	Display reads same as counter ± 0.01 kHz
19		Display		Switch between Range: 11 kHz and 110 kHz Freq Ranges		11 kHz Freq Range: 11.05 to 11.25 kHz. 110 kHz Freq Range: 110.5 to 112.5 kHz.	Set for best frequency balance between freq ranges. C44 (.001 μF nominal value) trims 11.00 kHZ range.
20	High Log			Freq Range: 11.00 kHz Lin/Log: Log	R31	11.15 kHz	
21	11:1 Frequency			Freq Range: 110 kHz Lin/Log: Lin Frequency Coarse knob: fully ccw	Verify only	10± 2kHz on display	
22	High Frequency Calibration			Frequency knobs: fully cw Freq Range: 1.1 MHz	C40	1.115 ±.005 MHz on display	C41 may be trimmed to obtain equal adjustment above and below 1.110 MHz
23				Frequency Coarse knob: fully ccw		Note display reading	
24				Freq Range: 11 MHz Frequency Coarse knob: fully ccw	C38	Set for 10 times reading noted in previous step	C39 may be trimmed to obtain equal adjustment above and below goal frequency
25				Frequency knobs: fully cw	R80	11.15 ±.05 MHz	
26	Amplitude	True rms Voltmeter		Func: ∿ Freq Range: 11.00 kHz Frequency Coarse fully ccw	R184	3.55 ±0.015 Vac (3.535 to 3.565 Vac)	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
27	Amplitude	True rms Voltmeter	Func Out (50Ω)	Func: ∿	R126	2.90 ±0.015 Vac (2.885 to 2.915 Vac)	
28				Frequency knobs: fully cw Freq Range: 1.1 kHz	R151		
29		dc Voltmeter		Freq Range: 110 mHz Func: ⊓⊔	R142	+5.025 ±0.025 Vdc. (+5.00 to 5.05 Vdc).	Turn frequency coarse knob fully ccw to hold each peak while adjusting
30					R147	−5.025 ±0.025 Vdc. (−5.00 to −5.05 Vdc).	
31	Waveform Quality and Frequency Response	Scope		Frequency knobs: fully cw Freq Range: 1.100 MHz Amplitude: 8Vp-p	R146	Minimum aberations <4% (320 mV)	Scope settings: 2V/div. 0.1 μs/div. (Observe peak-to-peak aberations at 0.5 V/div by adjusting vertical position)
32				Amplitude: fully cw		Rise/Fall <22 ns	Scope settings: X10 Magnification
33				Func: ∿ Frequency knobs: fully cw Freq Range: 11.00 MHz	Verify only	Amplitude between 8.6 and 10V	Scope settings: Magnification Off
34		Spectrum Analyzer		Freq Range: 1.100 MHz		Harmonics less than −40 dBc from 1.1 to 0.1 MHz	Rotate coarse frequency controls through its range and return fully cw
35				Freq Range: 11 MHz		Harmonics less than −28 dBc from 11 to 1 MHz	Rotate the Coarse frequency control through its range and return to full cw.
36	D.C. Offset	Scope or dc voltmeter		Function: ⎓ (dc) D.C. Offset: fully cw		Minimum +5Vdc	The calibration procedure is complete; start functional checkout.
37				D.C. Offset: ccw (not in detent)		Continuous dc level change to −5Vdc or more negative	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
38	– 20 dB Output	Scope	Func Out (50Ω)	D.C. Offset: Off Func: ⊓⊔ Frequency knobs: fully cw Freq Range: 11.00 kHz	Verify only	Approximately 10 Vp-p square wave	Scope settings: 2V/div. 20 μs/div.
39			Func Out (– 20 dB)			Approximately 1Vp-p square wave. Note value.	Scope settings: 0.2V/div.
40			Func Out (50Ω)	Amplitude: fully ccw		Verify Vp-p less than value noted in step 39	
41	Sync Out		Sync Out	Amplitude: fully cw		Normal TTL level square wave	Remove 50Ω termination. Scope setting: 2V/div.
42	Trigger and Gate			Mode: Trig		Display shows Trig (numbers blanked). Scope shows approxi- mately 0Vdc.	
43			Func Out (50Ω)	Func: ∿		Verify triggered sine wave	Connect 1kHz TTL signal from external source to CH2 and Trig In (TTL) BNC. Scope settings: 0.2 ms/div. Trigger on CH2, Monitor CH1
44				Mode: Gate		Display shows Gate Verify gated sine wave	
45	Manual Trigger					Sine wave when Trigger button pressed	Disconnect external sig- nal source, scope CH2 and Trig In (TTL). Trigger on CH1
46	VCG In			Mode: Cont Freq Range: 110.0 kHz Frequency knobs: fully ccw Func: ⊓⊔		Display shows 110 ± 5 kHz	Connect +5VDC to VCG In BNC.
47						Verify one cycle >5 divisions	Remove voltage from VCG In BNC. Scope setting: 2ms/div.
48	Linear Sweep	Scope	Func Out (50Ω), Swp Out	Frequency knobs: fully cw Freq Range: 110.0 kHz Func: ∿		CH2: >+5 Vdc	Scope — CH1: 2V/div; Func Out CH2: 2V/div; Swp Out. Time Base: 1ms/div. Trigger: – slope, CH2 Vert Mode: Alternative
49				Mode: Swp Set. Frequency knobs: fully ccw.		Display: Set. Scope: CH1 frequency and CH2 voltage varies in the Swp Set control.	

Table 5-1. **Calibration Procedure (Continued)**

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
50	Linear Sweep	Scope	Func Out (50Ω) Swp Out	Mode: Swp Swp Set: cw	Verify only	Display: Swp 0.01s Scope: CH2-0 to ⩾5 V, 10 ms ramp. CH1 Linear swept sine wave.	
51	Log Sweep			Lin/Log: Log		Display: Log. Scope: CH1 Logarithm swept sine wave.	
52	Sweep Time .1s			Swp Time: .1 sec		Display: 0.1 sec. Scope: CH2 0 to ⩾5 V, 100 ms ramp.	Scope: Time base: 10 ms/div. Vert Mode: Chop Sweep Mode: Norm Trig.
53	Sweep Time 1s	Scope and Counter		Swp Time: 1 sec		Display: 1s. Scope: Slow sweep. Counter: 1s period	Scope: Time base: 1ms/div. Trigger: CH1. Connect counter to Swp Out.
54	Sweep Time 10s			Sweep Time: 10s		Display: 10s. Scope: Slow sweep. Counter: 10s period.	
55	Triggered Sweep	Scope		Swp Time: 0.01s Lin/Log: Lin. Freq Range: 1.100 kHz. Mode: Trig Sweep Frequency Coarse: cw Fine: cw		Display: 0.01s. Trig Swp Scope: Sweep starts coincident with rising edge of trigger signal; waveform returns to baseline at end of sweep.	Disconnect counter; Connect pulse generator to CH2 and Trig In. Scope: CH1 and CH2: 2V/div. Time base: 5ms/div. Trigger: CH2; +Slope. Pulse Generator: TTL level. 5ms pulse at 40 Hz (25 ms) rate.
56						Scope: Sweep starts coincident with rising edge of trigger signal; waveform returns to start frequency.	Pulse Generator: 15 ms pulse at 40 Hz rate.

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
57	Stab	Scope		Mode: Cont Stab: Off Frequency Fine: initially centered Frequency Coarse: 500Hz Func: ⊓⊔ Stab: On	Verify only	Quickly turn Frequency Fine knob as indicated and verify the following: 1) Rotate the Fine control cw to move transition from center to 3cm to the left. 2) Transition travels approximately 2 cm toward center of scope display 3) Transition jumps back to 3cm left of center grid line 4) Stab now Off	Disconnect Trig In signal Scope settings: CH1: 2V/div. Time base: 0.2 ms/div. Trig: CH1, +Slope X10 Magnification: On Adjust horizontal position for square wave transition at center NOTE *Stabilizer automatically disengages when it reaches its electrical limits.*
58				Use Frequency Fine knob to return square wave transition to center vertical grid line Stab: On		Same as step 57 in opposite direction	Repeat as in step 57 except turn Frequency Fine knob ccw to move transition from center to 3 cm right
59	Low Frequency Ranges			Frequency knobs: fully cw		Display reads between 1.105 kHz and 1.125 kHz	Scope settings: 50 μs/div. X10 Magnification: Off Set horizontal variable for 1 cycle on screen
60				Freq Range: 110.0 Hz		Display reads between 110.5 Hz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5 ms/div.
61				Freq Range: 11.00 Hz		Display reads between 11.05 Hz and 11.25 Hz. Scope screen shows 1 cycle.	Scope setting: 5ms/div. Trigger mode: Normal
62				Freq Range: 1.100 Hz		Display reads between 1.105 Hz and 1.125 Hz. Scope screen shows 1 cycle.	Scope setting: 50 ms/div.
63				Freq Range: 110.0 mHz		Display reads between 110.5 mHz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5s/div.

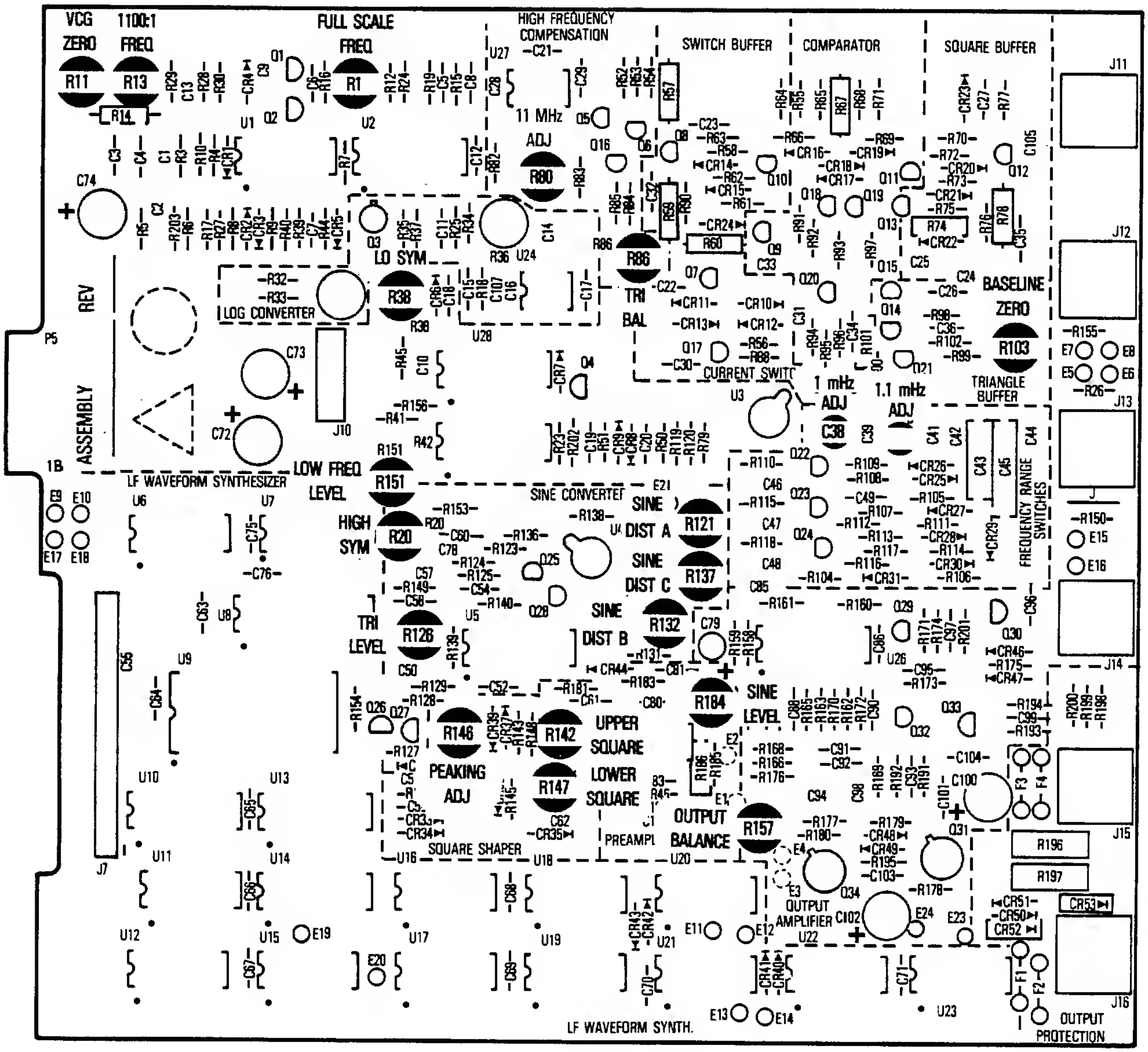


Figure 5-1. Calibration Points

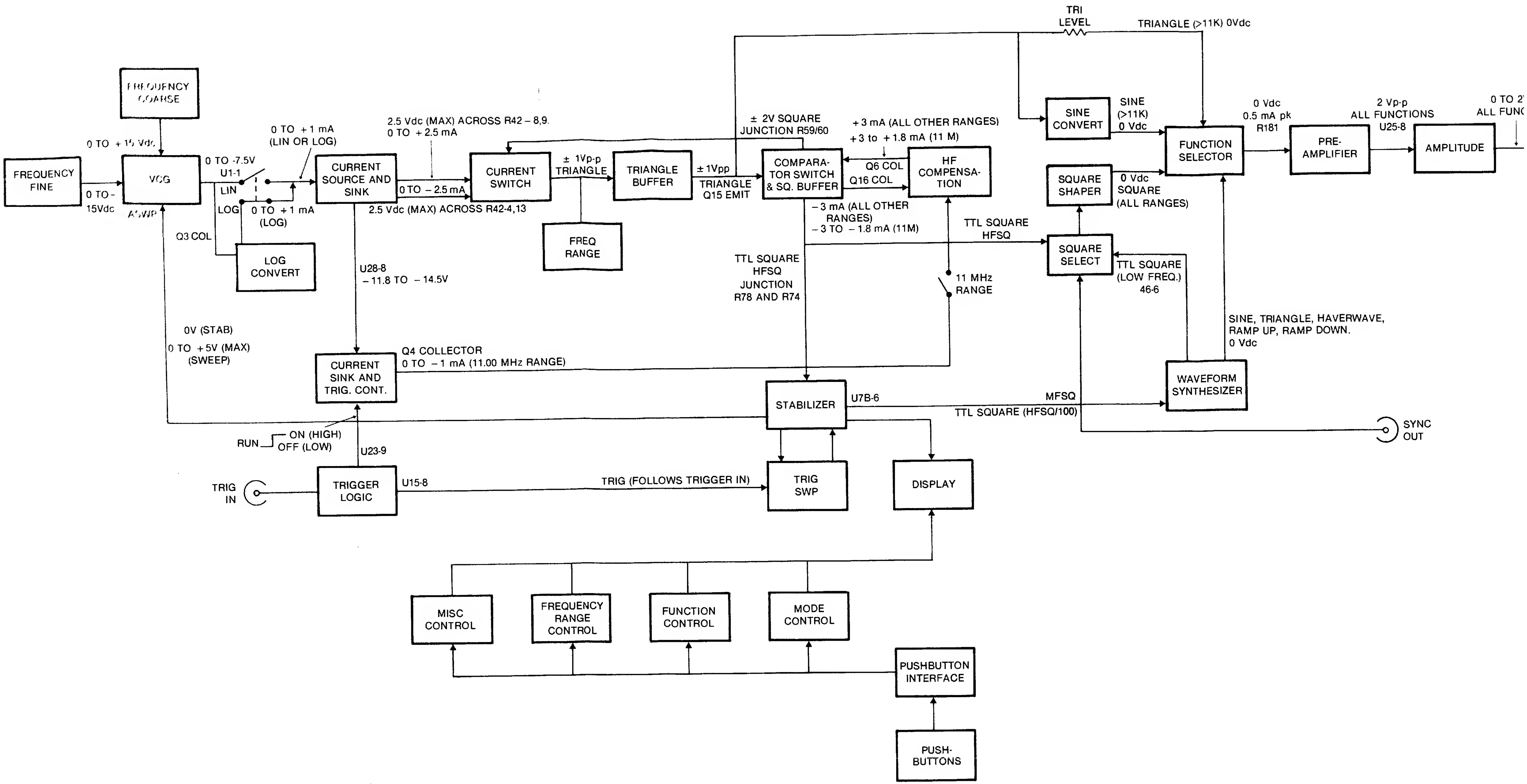
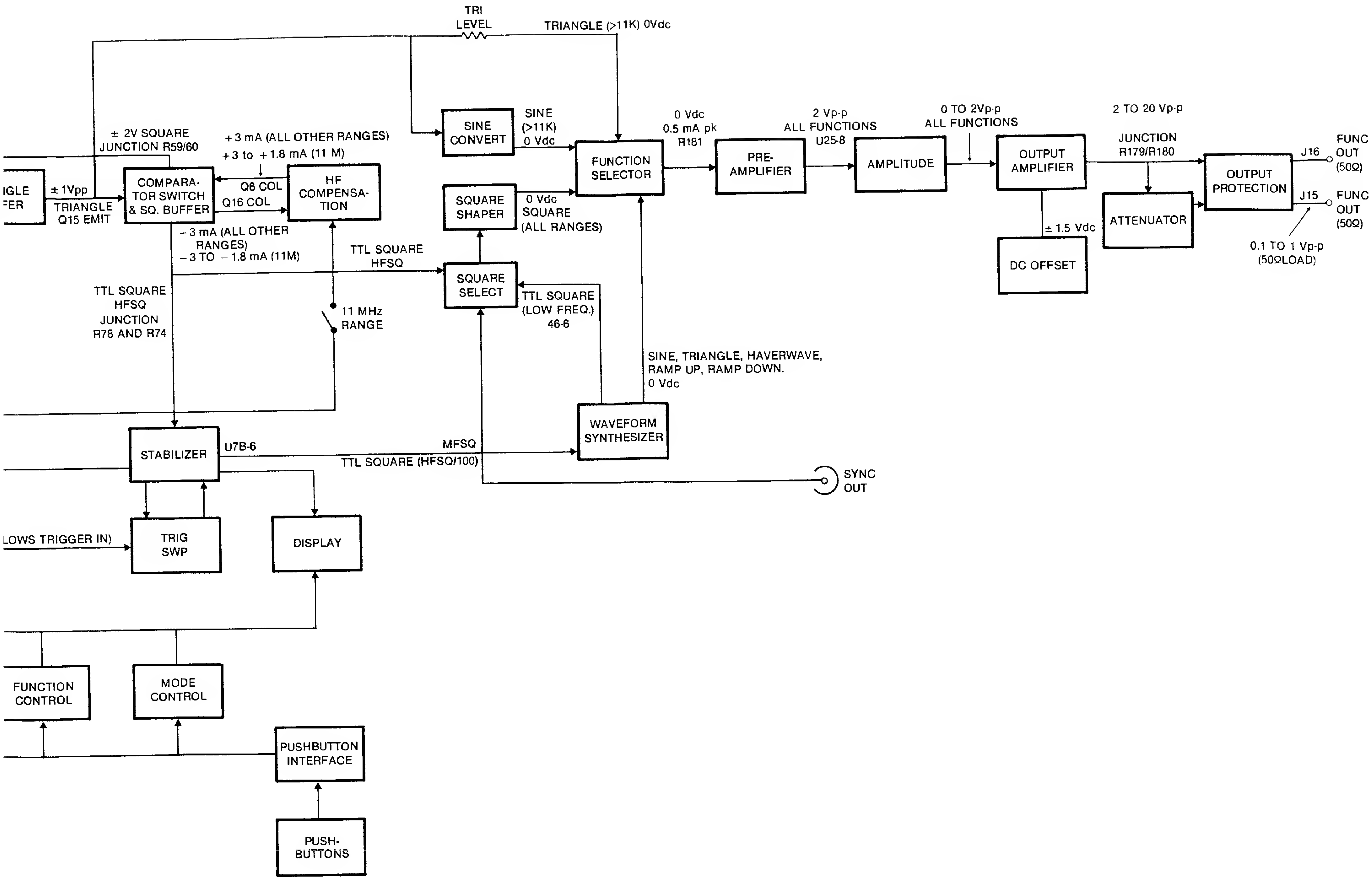


Figure 6-1. Troubleshooting Block Diagram


TRI
LEVEL
TRIANGLE (>11K) 0Vdc
SINE
CONVERT
SINE
(>11K)
0 Vdc
FUNCTION
SELECTOR
0 Vdc
0.5 mA pk
R181
PRE-
AMPLIFIER
2 Vp-p
ALL FUNCTIONS
U25-8
AMPLITUDE
0 TO 2Vp-p
ALL FUNCTIONS
OUTPUT
AMPLIFIER
2 TO 20 Vp-p
JUNCTION
R179/R180
OUTPUT
PROTECTION
J16
FUNC
OUT
(50Ω)
J15
FUNC
OUT
(50Ω)
0.1 TO 1 Vp-p
(50ΩLOAD)
ATTENUATOR
± 1.5 Vdc
DC OFFSET
± 2V SQUARE
JUNCTION R59/60
+3 mA (ALL OTHER RANGES)
+3 to +1.8 mA (11 M)
IGLE
FER
± 1Vpp
TRIANGLE
Q15 EMIT
COMPARA-
TOR SWITCH
& SQ. BUFFER
Q6 COL
Q16 COL
HF
COMPENSA-
TION
SQUARE
SHAPER
0 Vdc
SQUARE
(ALL RANGES)
−3 mA (ALL OTHER
RANGES)
−3 TO −1.8 mA (11M)
TTL SQUARE
HFSQ
SQUARE
SELECT
TTL SQUARE
(LOW FREQ.)
46-6
TTL SQUARE
HFSQ
JUNCTION
R78 AND R74
11 MHz
RANGE
SINE, TRIANGLE, HAVERWAVE,
RAMP UP, RAMP DOWN.
0 Vdc
WAVEFORM
SYNTHESIZER
STABILIZER
U7B-6
MFSQ
TTL SQUARE (HFSQ/100)
SYNC
OUT
LOWS TRIGGER IN)
TRIG
SWP
DISPLAY
FUNCTION
CONTROL
MODE
CONTROL
PUSHBUTTON
INTERFACE
PUSH-
BUTTONS

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration for repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description (Section 4) in conjunction with the schematics (Section 7). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as their relationship.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

The intent of this section is to provide the information required to return this instrument to proper operation. Information is divided into two parts. Part one contains the overall instrument troubleshooting block diagram (figure 6-1), which is useful in isolating defective blocks within the instrument. Part two consists of a series of circuit guides (paragraph 6.3), one for each block shown in figure 6-1, each guide provides settings and measurements for troubleshooting that block. Also, each circuit guide references related schematics, circuit descriptions, and calibration procedures.

Before beginning the troubleshooting process, verify the instrument's controls are set correctly. For example, the instrument cannot produce a 100 kHz ramp up. For more information about instrument operation, refer to section 3 of this manual.

Also, rule out calibration as a possible problem. For instance, if the 10 kHz triangle amplitude is out of specification while the sine and square amplitudes are in specification, then the TRI LEVEL pot (R126) quite possibly needs adjustment.

Finally, inspect the instrument's components, wiring, and circuit boards for heat damage.

6.2.1 Isolating a Problem

To successfully troubleshoot this instrument, the symptom must first be identified, the faulty block isolated, the block analyzed, and the defective component located and replaced.

To identify the symptom, use all the front panel controls and connectors. Pay particular attention to the frequency range as this identifies the signal flow (function generator loop or synthesizer).

Once the signal flow is established, figure 6-1 can be used to isolate the circuit block. Start measuring the outputs and inputs of the circuit blocks until the defective block is located.

Once the block is isolated, refer to the appropriate circuit guide; see table 6-1. Set the controls as instructed and take the measurements given to check out the block. Paragraph 6.4 gives component troubleshooting information.

6.3 TROUBLESHOOTING GUIDES

Table 6-1. Circuit Guides

Circuit Guide	Paragraph
VCG	6.3.1
Current Source and Sink	6.3.2
Current Sink and Trigger Control	6.3.3
Log Converter	6.3.4
Current Switch	6.3.5
Frequency Range Switches	6.3.6
Triangle Buffer	6.3.7
Comparator, Switch and Square Buffers	6.3.8
High Frequency Compensation	6.3.9
Trigger Logic	6.3.10
Waveform Synthesizer	6.3.11
Stabilizer	6.3.12

Table 6-1. Circuit Guides (Continued)

Circuit Guide	Paragraph
Trigger Sweep Logic	6.3.13
Square Selector	6.3.14
Square Shaper	6.3.15
Sine Converter	6.3.16
Function Selector	6.3.17
Preamplifier	6.3.18
Output Amplifier	6.3.19
Attenuator	6.3.20
Output Protection	6.3.21
Pushbutton Interface	6.3.22
Power-On Reset	6.3.23
Mode Control	6.3.24
Misc Control	6.3.25
Frequency Range Control	6.3.26
Function Control	6.3.27
Display	6.3.28
Power Supply	6.3.29

6.3.1 VCG

Related information in this manual
Schematic: 0103-00-1116 sheet 1.
Circuit Description: Paragraph 4.2.1.1.
Calibration Procedure: Table 5-1, Steps 11, 12, and 17.

Set the frequency controls as indicated in table 6-2 and take the measurements; the stabilizer must be off.

Table 6-2. VCG

Frequency Knobs	P5-B4	J7-2	U1-1	J13
Both full cw	+15V	0V	−7.5V	+5V
Both full ccw	+1.36V	−15V	~0V	~0V

Related digital control lines.
VCG KILL: TTL low = VCG In connected;
TTL high = VCG disconnected.

6.3.2 Current Source and Sink

Related information in this manual.
Schematic: 0103-00-1116 Sheet 1.
Circuit Description: Paragraph 4.2.1.1.
Calibration Procedure: Table 5-1, Steps 13, 15, and 16.

Set the controls as shown and make the checks in tables 6-3 and 6-4.

Control	Settings
VCG In	0V
Stab	Off
Frequency knobs	As directed
Freq Range	1.100 kHz

Table 6-3. Current Source

Frequency Knobs	U1-1	U1-9	U1-8	U28-14
Both full cw	−7.5V	0V	~1.3V	~+11.8V
Both full ccw	~0V	0V	~0.5V	~+14.5V

Table 6-4. Current Sink

Frequency Knobs	R42-16	R42-14	R42-3	U28-1
Both full cw	+2.5V	−2.5V	0V	−11.8V
Both full ccw	+2.26 mV	−2.26 mV	0V	~−14.5V

6.3.3 Current Sink and Trigger Control

Related information in this manual.
Schematic: 0103-00-1116 Sheet 1.
Circuit Description: Paragraph 4.2.1.1.

Set the controls as shown and perform the checks in tables 6-5 and 6-6.

Control	Settings
Frequency knobs	As directed
Lin/Log	Lin
Freq Range	1.100 kHz
VCG In	0V

Table 6-5. Current Sink and Trigger Control

Frequency Knobs	U28-1	U28-7
Both full cw	−11.8V	−12.5V
Both full ccw	~−14.5V	~−15V

Control	Settings
Frequency knobs	Both full cw
Frequency Range	1.100 kHz
VCG In	0V
Mode	As directed

Table 6-6. Trigger Control

Mode	RUN (U23-9)	Anode CR7	Cathode CR7
Cont	High	+2.1V	−0.7V
Trig	Low	−1.1V	−0.7V

6.3.4 Log Converter

Related information in this manual.
Schematic: 0103-00-1116 Sheet 1.
Circuit Description: Paragraph 4.2.1.2.
Calibration Procedure: Table 5-1, Steps 14 and 20.

Set the controls as shown; then perform the checks in table 6-7.

Control	Settings
Lin/Log	Log
Frequency knobs	As directed
VCG In	0V
Stab	Off

Table 6-7. Log Converter

Frequency Knobs	U1-1	U1-8	U24-2
Both full cw	−7.5V	∼+1.3V	0Vdc
Both full ccw	∼0V	∼0.5V	0Vdc

Related digital controls.
A TTL low at U2 pin 1 switches in the log converter.

6.3.5 Current Switch

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.3.

Set the controls as shown, and take the measurements as shown in figure 6-2.

Control	Settings
Frequency knobs	Both full cw
Freq Range	1.100 kHz
Stab	Off
Mode	Cont

6.3.6 Frequency Range Switches

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.4.
Calibration Procedure: Table 5-1, Steps 22 through 24.

The table 6-8 lists the logic levels for the nine frequency ranges. A low enables the range capacitor; a high disables the range capacitor. Table 6-9 gives measurement values for a single typical range switch ($\overline{FR6}$), these levels are typical of all three switches.

Table 6-8. Frequency Range Truth Table (TTL levels)

Range	$\overline{FR6}$	$\overline{FR5}$	$\overline{FR4}$
11.00 MHz	High	High	High
1.100 MHz	Low	High	High

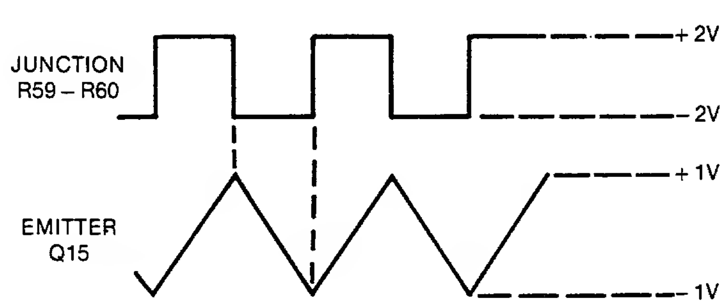


Figure 6-2. Current Switch Waveforms

Table 6-8. **Frequency Range Truth Table (TTL levels) (Continued)**

Range	$\overline{FR6}$	$\overline{FR5}$	$\overline{FR4}$
110.0 kHz	High	Low	High
11.00 kHz	High	High	Low
1.100 kHz	Low	High	High
110.0 Hz	High	Low	High
11.00 Hz	Low	High	High
1.100 Hz	High	Low	High
110.0 mHz	High	High	Low

Table 6-9. Frequency Range ($\overline{FR6}$ shown, typical)

$\overline{FR6}$	TTL Low	TTL High
Base Q22	+3.6 Vdc	+4.0 Vdc
Emitter Q22	+4.3 Vdc	+4.3 Vdc
Collector Q22	+4.0 Vdc	−15 Vdc
Junction R108 and R109	+1.4 Vdc	−15 Vdc
Junction R106 and R107	−7.5 Vdc	−7.5 Vdc

6.3.7 Triangle Buffer

Related information in this manual.
- Schematic: 0103-00-1116 Sheet 2.
- Circuit Description: Paragraph 4.2.1.5.
- Calibration Procedure: Table 5-1; Steps 5 and 10.

Set the controls as shown, and take the measurements as shown in figure 6-3 and table 6-10.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both full cw
Mode	As directed

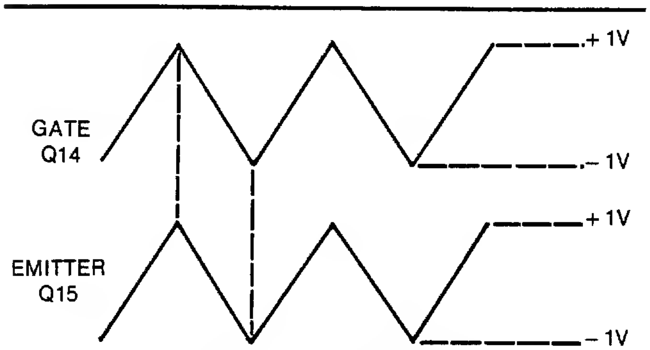


Figure 6-3. Triangle Buffer (Cont Mode)

Table 6-10. Triangle Buffer (Trigger Mode)

Test Point	Desired Results
Gate Q14	0Vdc
Source Q14	+0.7V
Base Q21	−5V
Emitter Q15	0Vdc

6.3.8 Comparator, Switch and Square Buffers

Related information in this manual.
- Schematic: 0103-00-1116 Sheet 2.
- Circuit Description: Paragraphs 4.2.1.6, 4.2.1.7, and 4.2.4.1.

Set the controls as shown; then take the measurements as shown in figure 6-4.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both full cw

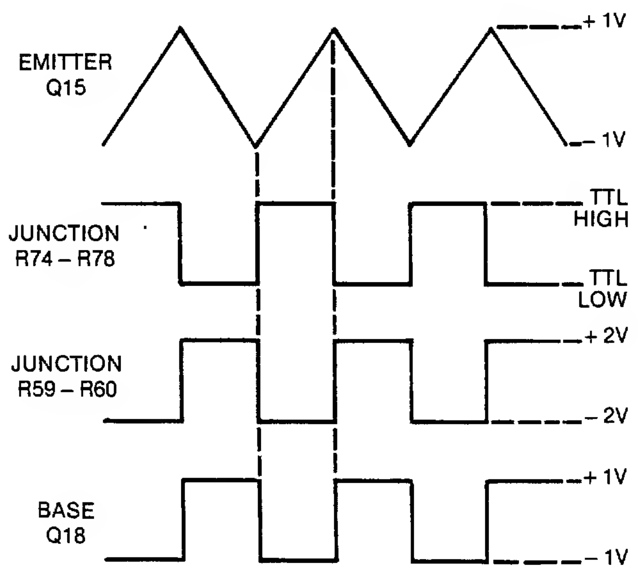


Figure 6-4. Comparator, Switch and Square Buffer

6.3.9 High Frequency Compensation

Related information in this manual.
- Schematic: 0103-00-1116 Sheet 2.
- Circuit Description: Paragraph 4.2.1.8.
- Calibration Procedure: Table 5-1, Steps 6 and 25.

Set the controls as shown, and then take the measurements as shown in tables 6-11 and 12.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both full cw

Table 6-11. Low Frequency Check

Test Point	Desired Results
U27-3	0Vdc
U27-2	0Vdc
U27-6	+0.7Vdc
Collector Q5	+10 Vdc
Base Q16	−10 Vdc
Emitter Q6	+10.7 Vdc
Emitter Q16	−10.7 Vdc

Table 6-12. High Frequency Compensation (11 MHz Range)

Select the 11 MHz range.

Test Point	Desired Results
U27-3	−5Vdc
U27-6	−4.3 Vdc
Collector Q5	+11.7 Vdc
Base Q16	−11.7 Vdc
Emitter Q6	+12.4 Vdc
Emitter Q16	−11.4 Vdc

Related digital control logic.

$\overline{\text{FR7}}$ goes low on the 11 MHz range;
$\overline{\text{FR7}}$ remains high on all other ranges.

6.3.10 Trigger Logic

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.1.9.

Table 6-13 lists the control lines relatedot the trigger logic circuit.

Table 6-13. Control Lines

Control Line	Description
Trig In	External trigger input signal.
Man Trig	Front panel manual trigger. Goes low when pushbutton is pressed.

Table 6-13. Control Lines (Continued)

Contol Line	Description
MC0	A control line from the mode control logic. Triggered Sweep, Trigger, and Gate modes: TTL high. Continuous, Sweep Set, and Sweep modes: TTL low.
MC1	A control line from the mode control logic. Gate, Continuous, and Sweep modes: TTL high. Trigger, Sweep Set, and Triggered Sweep modes: TTL low.
$\overline{\text{KILL}}$	A control line from the function control logic. This line goes low when the dc function is selected. The line remains high for all other functions.
$\overline{\text{SWPRUN}}$	A control line from the trigger sweep logic. A low enables the RUN line. A high disables the RUN line.
HFSQ	TTL level square wave from the function generator loop.
LF	A control line from the frequency range control logic. 11 MHz, 1.1 MHZ, 110 kHz, 11 kHz ranges: TTL low; all other ranges: TTL high.
TRIG	A signal line which drives the trigger sweep logic. Its signal follows Trig In or Man Trig signals.
RUN	A control line that enables or disables the function generator loop. A TTL low turns the generator off, and a TTL high turns the generator on.

6.3.11 Waveform Synthesizer

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.2.

Before troubleshooting the waveform synthesizer, review the circuit description (paragraph 4.2.2) and use the following hints. Remember the waveform synthesizer produces waveforms on the 1.100 kHz and below ranges.

1. Check the counter's clock input: U15-11, U14-2, U10-2. EFC is always a TTL high.
2. Verify the up/down counter's data lines change with each clock pulse: U6-3, U14-14, U14-13, U14-12, U14-11, U10-14, U10-13, U10-12, U10-11.

3. Verify the up/down control lines switch coincident with the positive and negative peaks: U17-11, U17-8, U10-1, U14-1.
4. Verify data lines from EPROM (U9) change. Also verify correct waveform selection using FS0 and FS1.

Function	**FS0**	**FS1**
DC	0	0
Sine	0	0
Triangle	0	1
Ramp Up	1	0
Ramp Down	1	1

5. Verify the data lines from the latch (U8) change.
6. Check U7 pin 4 for the correct waveform.
7. Check $\overline{\text{SYNTH}}$ (U5-16) for a low.

6.3.12 Stabilizer

Related information in this manual.
Schematic: 0103-00-1115 Sheets 2 and 3.
Circuit Description: Paragraph 4.2.3.

The circuit description's text, tables, and figures contains the necessary information to troubleshoot the stabilizer circuit.

6.3.13 Trigger Sweep Logic

Related information in this manual.
Schematic: 0103-00-1115 Sheet 3.
Circuit Description: Paragraph 4.2.3.6.
Table 6-14 lists the control lines used in the trigger sweep logic.

Table 6-14. Trigger Sweep Logic

Control Line	Function
Trig	Trigger input, either manual or external trigger.
$\overline{\text{SWPRUN}}$	Controls the function generator loop. A low enables the generator. A high disables the generator.
UNSTAB	Clocks in the TRIG signal. Originates from $\overline{\text{FRCHG}}$ and is disabled except when the Up/Down counter (U8F) reaches a terminal count.
SWP	From mode control logic, Low during Cont, Trigger, and Gate modes; high during Sweep Set, Sweep, and Trig Sweep.
CONT	From mode control, high during Continuous mode; low during all other modes.

Table 6-14. Trigger Sweep Logic (Continued)

Control Line	Description
MC0	From mode control, high during trigger, gate, and trig Sweep modes; low during Continuous, Sweep Set, and Sweep modes.

6.3.14 Square Selector

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.2.

Set the controls as shown; then take the measurement as shown in table 6-15.

Control	**Settings**
Freq Range	As specified
Frequency knobs	As desired
Mode	Cont

Table 6-15. Square Selector Measurements

Frequency Range	LF Control Line	Square Source	TTL SQ (Output)
⩾11.00 kHz	Low	HFSQ (Function Generator Loop)	Square wave in phase HFSQ
<11.00 kHz	High	U6-6 (LFSQ) (Waveform Synthesizer)	Square wave in phase with LFSQ

6.3.15 Square Shaper

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.3.
Calibration Procedure: Table 5-1, Steps 29 through 31.

Set the controls as shown, and take the measurements shown in figure 6-5.

Control	**Settings**
Power	Turn Off; then On
Frequency knobs	Both full cw
Function	⊓⊔ (Square)
Mode	Cont

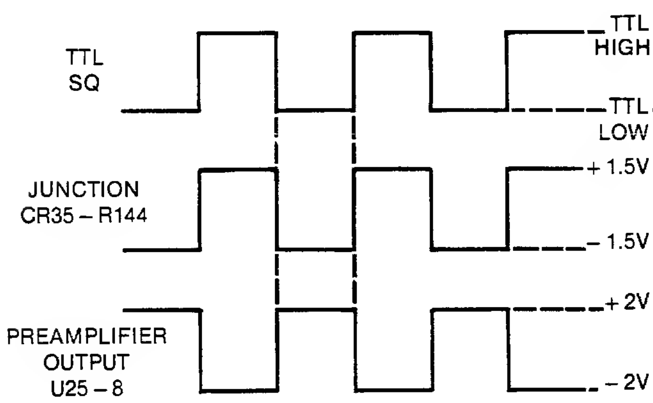


Figure 6-5. Square Shaper

6.3.16 Sine Converter

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.4.
Calibration Procedure: Table 5-1, Step 17.

Set the controls as shown, and take the waveform measurements as shown in figure 6-6.

Control	Settings
Frequency knobs	As desired
Freq Range	⩾11.00 kHz
Mode	Cont
Function	∿ (Sine)

NOTE

Time symmetry and dc offset of triangle affects the sine distortion; refer to the calibration procedure, steps 12 to 15.

On the 1.100 kHz range and below, the waveform synthesizer creates the sine wave. Thus, the sine converter has no affect on the lower five frequency ranges.

6.3.17 Function Selector

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.5.

The function selector, which consists of four switches, routes the various functions to the preamplifier; only one switch will be closed at a time. Table 6-16 describes the function selector control lines. A low logic level closes the respective switch. All control lines originate at the function control logic circuit.

Table 6-16. Function Selector Control Lines

Control Line	Description
$\overline{\text{SYNTH}}$	At frequencies below the 11.00 kHz range, selects signals from waveform synthesizer.
$\overline{\text{SQR}}$	At frequencies on or above 11.00 kHz range, selects square wave.

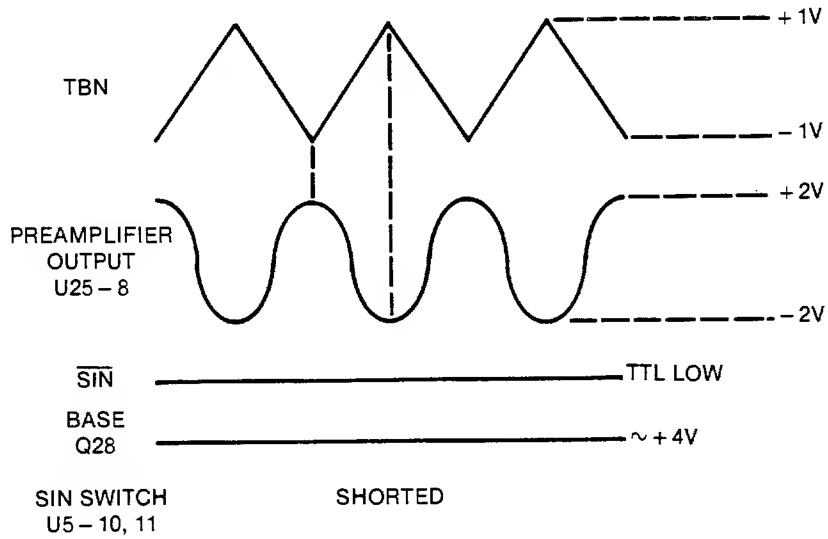


Figure 6-6. Sine Converter

Table 6-16. Function Selector Control Lines (Continued)

Control Line	Description
$\overline{TRI}$	At frequencies above on or 11.00 kHz range, selects triangle wave.
$\overline{SIN}$	At frequencies on or above 11.00 kHz range, selects sine wave.

6.3.18 Preamplifier

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.6.
Calibration Procedure: Table 5-1, Step 26.

DC Problems

Set the controls as shown; then perform the checks in table 6-17.

Control	Settings
Function	— — — — (DC)
DC Offset	Off

Table 6-17. Preamplifier

Test Point	Desired Results
U25 pin 14	0 ± .02Vdc
E1	0 ± .05Vdc

Function Problems

Set the controls as shown, and measure the waveform at E1: ±2V sine wave.

Control	Settings
Power	Turn Off; then On
D.C. Offset	Off
Amplitude	Full cw

6.3.19 Output Amplifier

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.7.
Calibration Procedure: Table 5-1, Step 9.

Set the controls as shown; then take the waveform measurements. Refer to table 6-18.

Control	Settings
Function	DC
D.C. Offset	Off

Table 6-18. Output Amplifier

Test Point	Desired Results
Junction R179 and R180	~0Vdc
Junction R166 and R190	~0Vdc
P5 pin B8	0Vdc
Junction R172 and R169	+14 Vdc
Junction R192 and R169	−14 Vdc
Across R165	14.3 Vdc
Across R171	1.5 Vdc
U26 pin 10	+12.8 Vdc
U26 pin 13	+12.8 Vdc
U26 pin 7	+5.7 Vdc

6.3.20 Attenuator

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.8.
Calibration Procedure: Table 5-1, Step 38.

Set the controls as shown; then take the waveform measurements. Refer to figure 6-7.

Control	Settings
Power	Turn Off; then On
D.C. Offset	Off
Amplitude	Full cw

Terminate the Function Out (−20 dB) with 50Ω load.

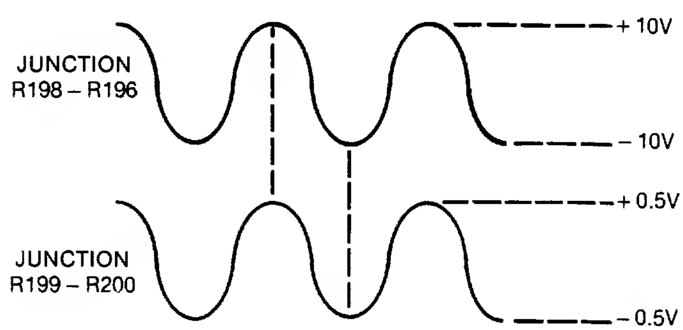


Figure 6-7. Attenuator

6.3.21 Output Protection

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.9.

Set the controls as shown; make the following checks.

Control	Settings
Power	Turn Off; then On
Amplitude	Full cw
D.C. Offset	Off

Note

Power must be turned off before checking fuses and diodes.

Check fuses (F1, F2) if there is no output at the Function Out (50Ω) BNC. Check for shorted diodes (CR50, CR51, CR2, CR3) if the fuses are ok. Check fuses (F3, F4) if there is no output at the Function Out (− 20 dB) BNC.

6.3.22 Pushbutton Interface

Related information in this manual.
Schematic: 0103-00-1115 Sheet 1.
Circuit Description: Paragraph 4.2.5.

Check the pushbutton interface circuit by pressing the appropriate front panel pushbutton and making the checks: refer to table 6-19.

Table 6-19. Pushbutton Interface

Pushbutton	Logic Level (TTL)	Interface	Logic Level (TTL)	Control Line
Trigger	high	U3G-8	low	MAN TRIG
Stab	low	U3G-2	high	STABPB
Function ←	low	U2G-8	high	FUNCDN
Function →	low	U2G-6	high	FUNCUP
Mode ←	low	U2G-10	high	MODDN
Mode →	low	U2G-12	high	MODUP
Freq Range ←	low	U2G-2	high	FRDN
Freq Range →	low	U2G-4	high	FRUP
Swp Time	high	U3G-10	low	SWPSPD
Lin/Log	low	U3G-6	high	LIN/LOG

6.3.23 Power-On Reset

Related information in this manual.
Schematic: 0103-00-1115 Sheet 1.
Circuit Description: Paragraph 4.2.6.1.

Turn the power off. Wait about one minute; then turn the power on. Take the waveform measurements as shown in figure 6-8 as power is being turned on.

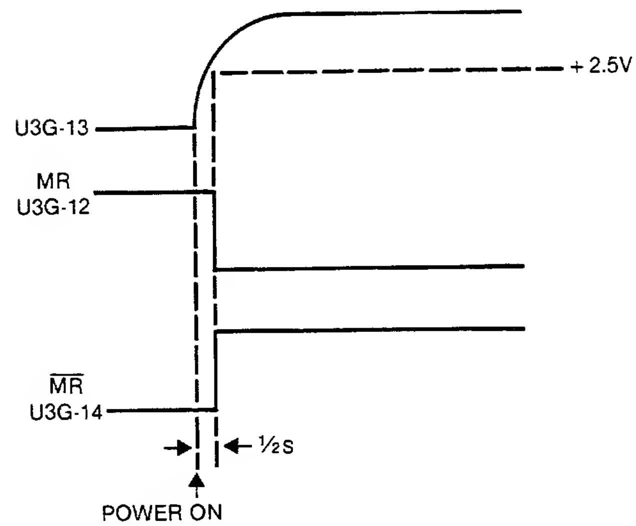


Figure 6-8. Power-On Reset

6.3.24 Mode Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.2.

Set the instrument to the desired mode. Compare the logic levels as shown in table 6-20.

6.3.25 Misc Control

Related information in this manual
Schematic: 0103-00-1115 Sheet 2.

Table 6-20. Mode Control Truth Table

Mode	U4G QD	U4G QC	U4G QB	U4G QA	MC0	MC1	SWPT	$\overline{SWP}$	SWP	$\overline{GATE}$	$\overline{TRIG}$	$\overline{CONT}$	$\overline{STOP}$	$\overline{CSWP}$	$\overline{TSWP}$	BL (2)
Gate	0	1	0	1	1	1	0	1	0	1	1	1	1	1	1	1
Trig	0	1	1	0	1	0	0	1	0	1	0	1	1	1	1	1
Cont (1)	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	0
Swp Set	1	0	0	0	0	0	1	0	1	1	1	1	0	1	1	0
Sweep	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	1
Trig Swp	1	0	1	0	1	0	1	0	1	1	1	1	1	1	0	1

Notes
1 Power-On Reset mode
2 Assumes EFC = 1

Table 6-21. Frequency Range Control

Max (Hz)	U6E QD	QC	QB	QA	LF	÷100	FR4	FR5	FR6	$\overline{FR7}$	DDP1	DDP2	$\overline{DDP3}$	DMHz	DK	DHz	DmHz	Actual Gen Freq
11.00M	1	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	11 M
1.100M	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	1	1.1 M
110.0k	0	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	1	110 k
11.00k(1)	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1	1	1	11k
1.100k	0	1	0	1	1	1	0	0	1	1	1	0	1	0	1	1	1	1.1M
110.0k	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	1	1	110k
11.00	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1.1M
1.100	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	110k
110.0m	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	11k

Note
1 Power-On Reset mode.

Circuit Description: Paragraph 4.2.6.3.

The circuit description's text contains the necessary information to troubleshoot the misc circuit.

6.3.26 Frequency Range Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.4.

Set the instrument to the desired frequency range and check the logic level as shown in table 6-21.

6.3.27 Function Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.5.

Set the controls as shown and check the logic levels as shown in table 6-22.

Control	**Settings**
Freq Range	11.00 kHz
Function	As needed

Table 6-22. Function Control

Function	U5D QD	QC	QB	QA	FS0	FS1	$\overline{SIN}$	$\overline{TRI}$	$\overline{SYNTH}$				$\overline{KILL}$		
DC	0	0	1	1	0	0	1	1	1	1	1	1	0	1	1
Sine	0	0	1	0	0	0	0	1	0	1	1	0	1	1	1
Square	0	0	0	1	0	0	1	1	1	1	0	1	1	1	1
Triangle	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1
Ramp Up	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0
Ramp Dn	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1

Notes
1 For this table LF = 0.
2 LF = 1 for Ramp Up and Ramp Down.
3 If LF = 1 (high) then $\overline{SIN}$ and $\overline{TRI}$ always high and $\overline{SYNTH}$ always low.
4 Power-On Reset condition, except $\overline{SIN}$ high and $\overline{SYNTH}$ low.

6.3.28 Display

Related information in this manual.
Schematic: 0103-00-1117.
Circuit Description: Paragraph 4.2.7.

Figure 6-9 illustrates a typical display segment while table 6-23 identifies the annunciators and thier control lines. The voltage between the control line and BL must be 5Vrms.

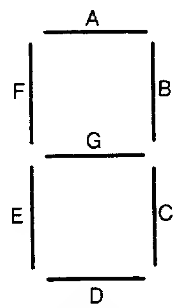


Figure 6-9. Typical Digit Segment Assignments

6.3.29 Power Supply

Related information in this manual.
Schematic: 0103-00-1113.
Circuit Description: Paragraph 4.2.8.
Calibration Procedure: Table 5-1, steps 1 through 4.

1. For fuse replacement, refer to paragraph 2.2.3.
2. To determine a faulty power supply, check for the voltages given in table 6-24.
3. If the pass devices' input tests bad, remove power and connector J3. Check for:
   (a) Blown fuse.
   (b) Shorted or open diodes (CR1, CR2).
   (c) Shorted or open capacitors (C2, C3, C4, C5, C10, C11) at the input the pass devices.
   (d) Short between the pass devices' metal mounting tab and chassis ground.
   (e) Bad transformer.
4. If the regulators input is good, remove power and connectors J4 and J5. Check for:
   (a) Shorted capacitors at the regulator's output.
   (b) Short between pass devices' mounting tab and chassis ground.
   (c) Excessive loading by board circuits; to verify, disconnect by removing either J4 or J5.
   (d) Check +15V and −15V pass devices for normal transistor operation.
   (e) If all of the above conditions appear normal, replace the voltage regulator; VR1 for +5V and VR2 for +15V and −15V.

Table 6-23. Display Control Lines

Display	Control Line
1st Digit	1 B/C
2nd Digit	2A, 2B, 2C, 2D, 2E, 2F, 2G
3rd Digit	3A, 3B, 3C, 3D, 3E, 3F, 3G
4th Digit	4A, 4B, 4C, 4D, 4E, 4F, 4G
k	K
Hz	Hz
MHz	MHz
mHz	mHz
Stab On	X1
Stab Off	X2
Gate Mode	Z1
Trig Mode	Z2
Cont Mode	Z3
DC Function	Z7
Sine Function	Z8
Square Function	Z9
Triangle Func	Z10
Ramp Up	Z11
Ramp Down	Z12
1st Dec Pt	DP1
2nd Dec Pt	DP2
3rd Dec Pt	DP3
Lin	X3
Log	X4
.01 Swp	X5
.1 Swp	X6
1 Swp	X7
10 Swp	X8

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than 1V is measured across its base-emitter junction in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage across the base-emitter junction.
3. If the collector an emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage or reversed bias, the transistor is defective.
4. In a transistor differential pair (common emitter stages), either their base voltages are the same in

Table 6-24. Power Supply

Supply	Voltage Tolerance	Test Point	Maximum Input Ripple	Test Point	Maximum Output Ripple	Test Point
+15V	±350 mV	C7	3Vac	C2	0.02Vac	C7
−15V	±350 mV	C8	3Vac	C3	0.02Vac	C8
+5V	±250 mV	C12	3Vac	C10	0.02Vac	C12

normal operating condition, or the one with less forward voltage across its base-emitter junction should be off (no collector current); otherwise one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than 1V (typically 0.7V) forward voltage across it.

6.4.3 Operational Amplifier

1. Generally the "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operation amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No measurable gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective. Gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485 and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

SECTION 7
PARTS LIST AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below. Special-order and option drawings, if any, will follow these standard drawings.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, and unit serial number.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Model 22 Assembly Drawing and Parts List	1000-00-1121
Instrument Outline Drawing	0002-00-1111
Instrument Schematic	0004-00-1111
Stabilizer Control Board Schematic	0103-00-1115
Stabilizer Control Board Assembly	1100-00-1123
Stabilizer Control Board Parts List	1100-00-1123
Waveform Generator Board Schematic	0103-00-1116
Waveform Generator Board Assembly	1103-00-1124
Waveform Generator Board Parts List	1100-00-1124
Front Panel Assembly and Parts List	1101-00-1122
Display Schematic	0103-00-1117
Display Assembly and Parts List	1208-00-1117
Power Supply Schematic	0103-00-1113
Power Supply Assembly and Parts List	1101-00-1113
Power Supply Board Assembly and Parts List	1208-00-1118
AC Primary Board Assembly and Parts List	1208-00-1119

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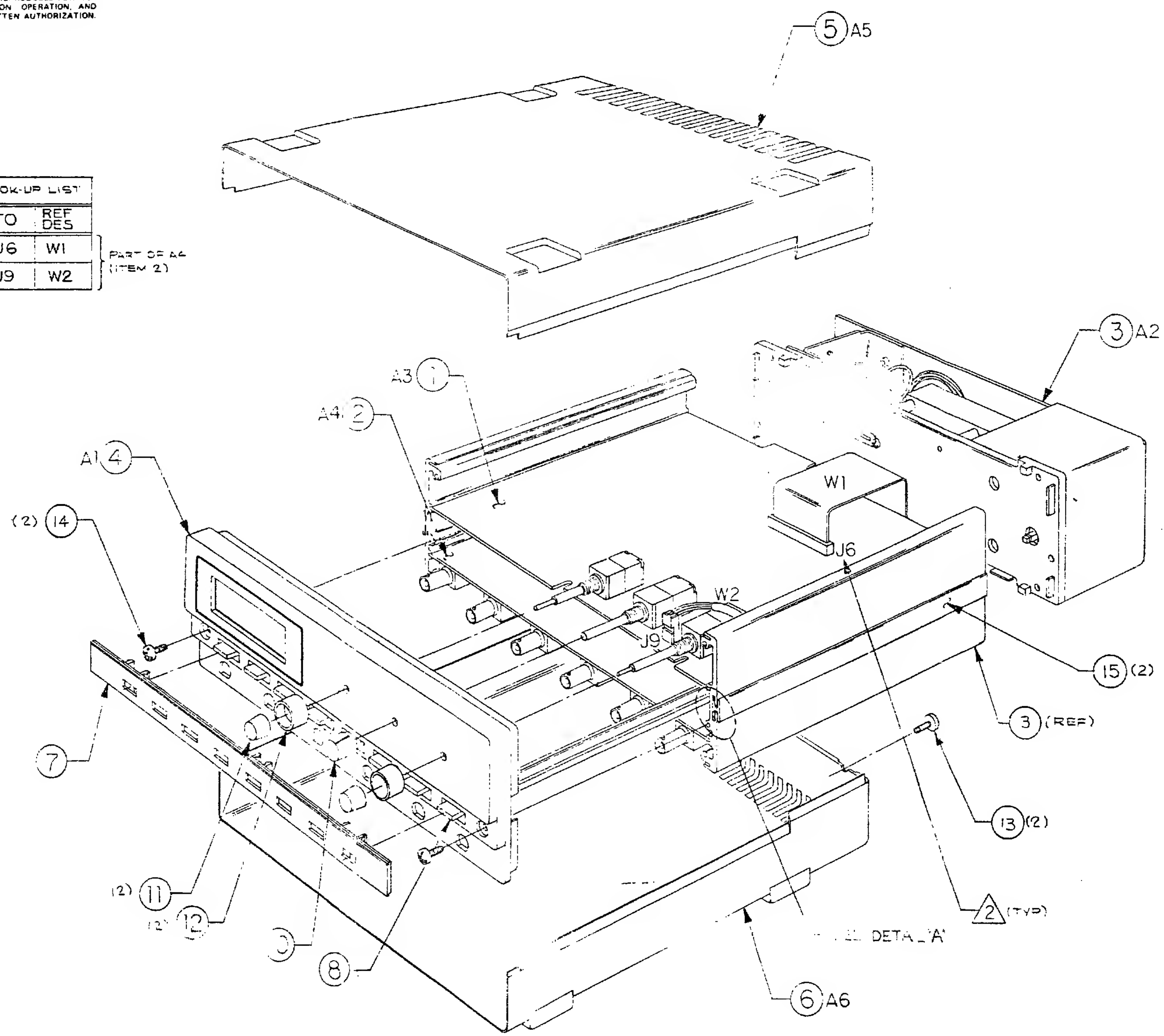
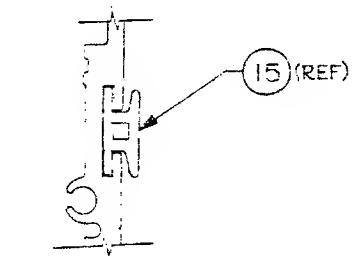
REV	ECN	BY	DATE	APP
B	ECN 4148			
D	4611		11/20/85	
E	4881			
F	6137			
G	7459			
H	[illegible]			

CABLE HOOK-UP LIST

FROM	TO	REF DES
P6	J6	W1
P9	J9	W2

PART OF A4 (ITEM 2)





DETAIL "A"
(SCALE: 2/1)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	ENGINEERING SPECIFICATIONS	0000-00-1121	WVTK	0000-00-1121	1
NONE	OUTLINE DRWG, INST	0002-00-1111	WVTK	0002-00-1111	1
NONE	SCHEMATIC, INST	0004-00-1111	WVTK	0004-00-1111	1
NONE	CALIB PROCEDURE	0006-00-1121	WVTK	0006-00-1121	1
NONE	ACCEPTANCE TEST SPECIFICATION	1002-00-1121	WVTK	1002-00-1121	1
1	PCA, STAB /CONTROL	22-1123	WVTK	1100-00-1123	1
2	PCA, WAVEFORM GEN	22-1124	WVTK	1100-00-1124	1
3	ASSY, POWER SUPPLY	21-1113	WVTK	1101-00-1113	1
4	ASSY, FRONT PANEL (MODEL 22)	22-1122	WVTK	1101-00-1122	1
5	ASSY, TOP COVER	21-1114	WVTK	1201-00-1114	1
NONE	ASSY, BOTTOM COVER	1206-00-1301	WVTK	1206-00-1301	1
NONE	ASSY, CABLE KIT	21-1120	WVTK	1207-00-1120	1
7	BEZEL, KEY(MODEL 22)	22-6170	WVTK	1400-01-6170	1
8	POWER ROD	21-6201	WVTK	1400-01-6201	1
15	INSERT, SIDE PANEL	20-7910	WVTK	1400-01-7910	2
10	KNOB, GRAY, SMALL W/LINE, 1/4 BUSHING	2400-01-0031	WVTK	2400-01-0031	1
11	KNOB, GRAY, SMALL 1/8 BUSHING	2400-01-0032	WVTK	2400-01-0032	2
12	KNOB, GRAY, CONCENTRIC OUTER	2400-01-0034	WVTK	2400-01-0034	2
13	SCREW, 10-32X1/2, TRS HD, Z	10-32X1/2 TRS PLPS MS	CMRCL	2800-20-0208	2
14	SCREW, 8X5/8 PHP, SMS, TYPE B	8-18 X 5/8	CMRCL	2800-22-8910	2
NONE	101-18 INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
NONE	PWR CORD	17251	BELDN	6001-80-0005	1

WAVETEK PARTS LIST	TITLE MODEL 22, 11MHZ STAB SWEEP/FUNCTION GENERATOR	ASSEMBLY NO. 1000-00-1121 PAGE 1	REV H

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. SEE 0004-00-1111 FOR INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN TALMADGE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR	TITLE MODEL 22, 11 MHz STAB. SWEEP/FUNCTION GEN
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030	MODEL NO 22
	DO NOT SCALE DWG	DWG NO 1000-00-1121 REV H
	SCALE NONE	CODE IDENT 23338 SHEET 1 OF 1

1000-00-1121 H

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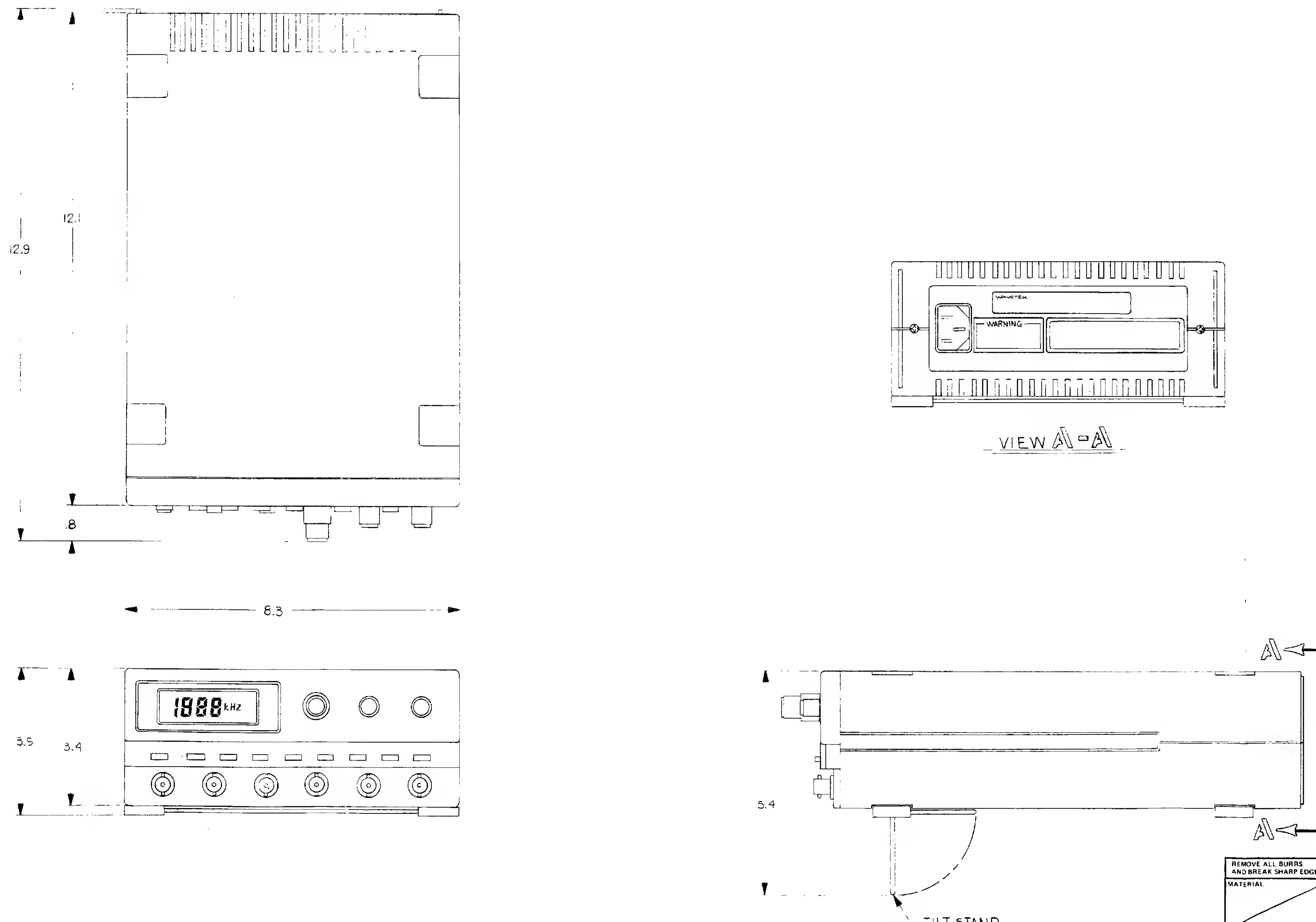

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. Magnolia	DATE 6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE OUTLINE DRAWING INSTRUMENT
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 21/22 · DWG NO 0002-00-1111 · REV
	SCALE 3/4 = 1		CODE IDENT 23338 · SHEET 1 OF 1

0002-00-1111

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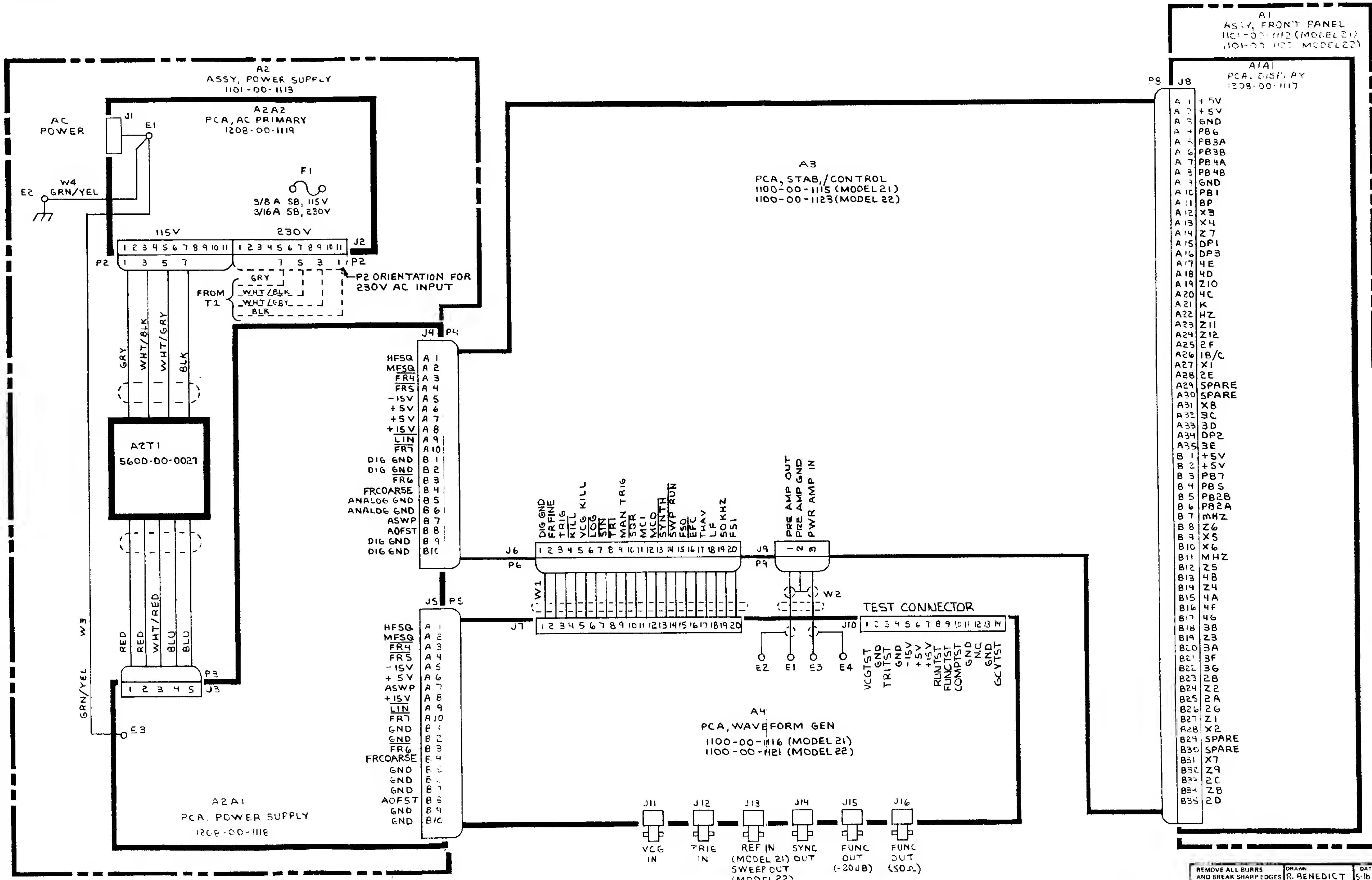

1000-00-1111 (MODEL 21)
1000-00-1121 (MODEL 22)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-18-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	RELEASE APPROV		TITLE SCHEMATIC, INSTRUMENT
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG	MODEL NO 21 / 22	DWG NO 0004-00-1111
	SCALE	CODE IDENT 23338	SHEET 1 OF

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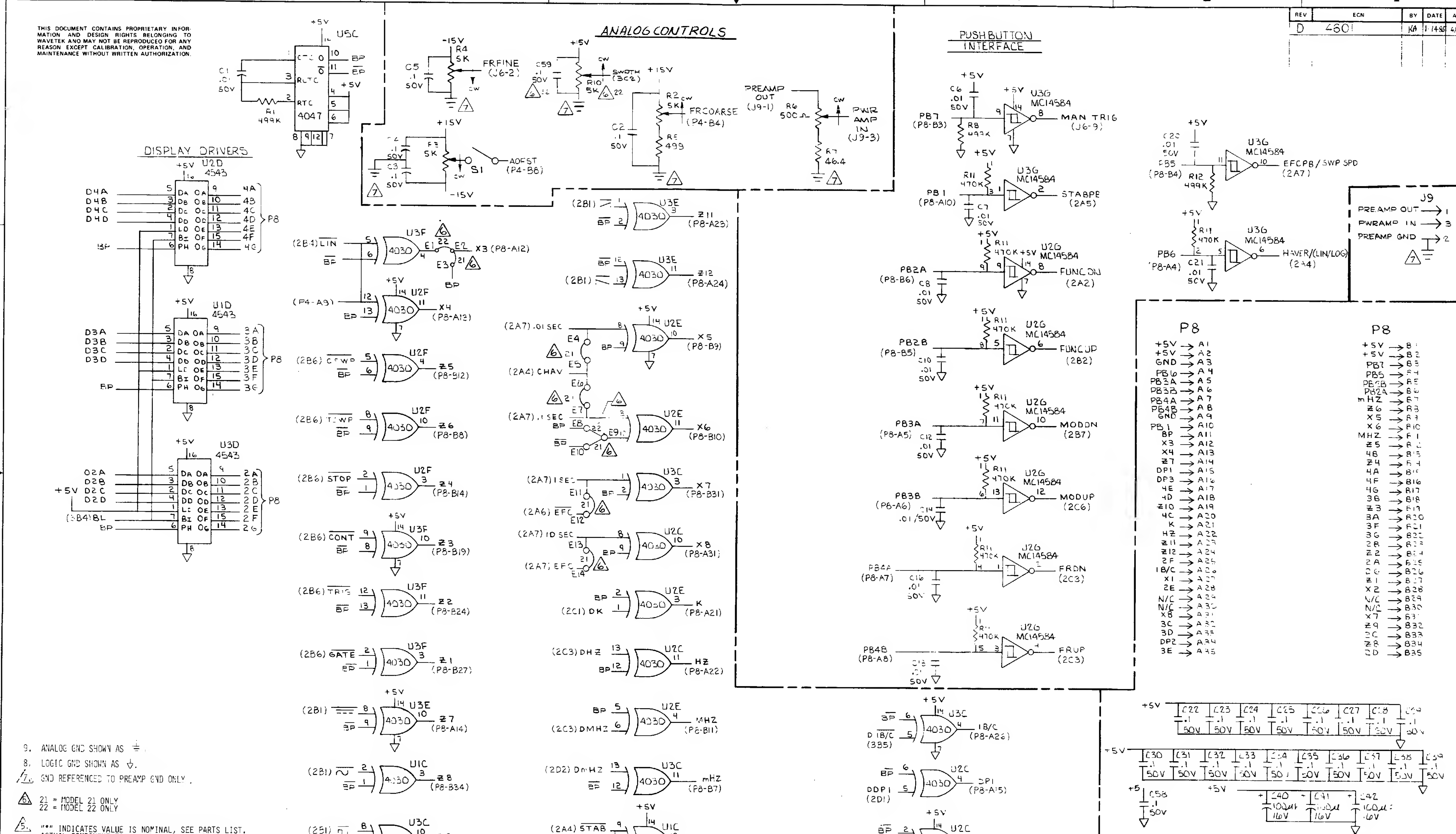


9. ANALOG GND SHOWN AS ⏚.
8. LOGIC GND SHOWN AS ⏚.
7. GND REFERENCED TO PREAMP GND ONLY.
6. 21 = MODEL 21 ONLY
   22 = MODEL 22 ONLY
5. "*" INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
4. CAPACITOR VALUES ARE IN MICROFARADS (μF).
3. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.
2. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111
1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A3.

NOTE: UNLESS OTHERWISE SPECIFIED

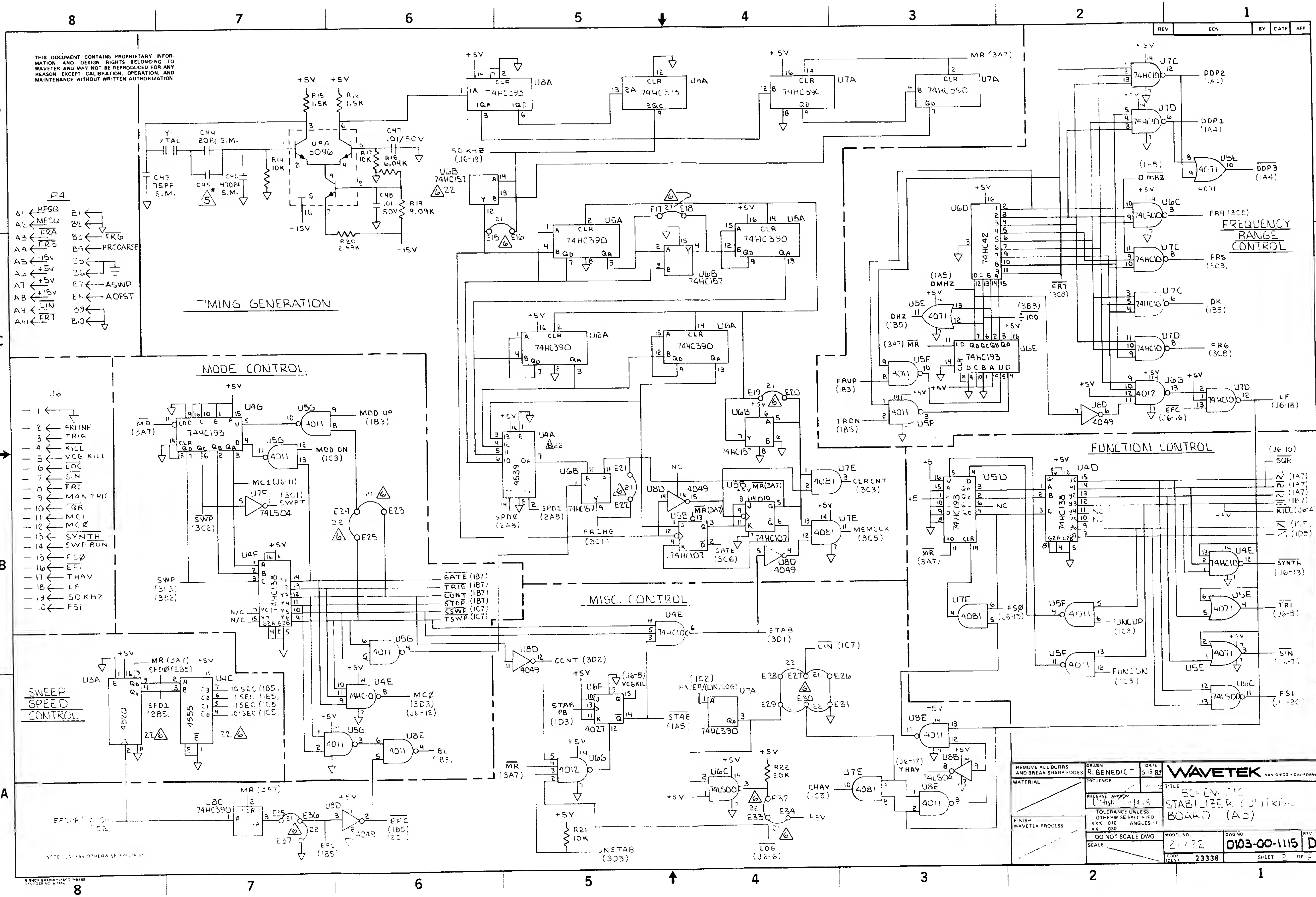
REV	ECN	BY	DATE	APP
D	4601	KA		

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN R. BENEDICT
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC STABILIZER CONTROL BOARD (A3)

MODEL NO 21/22 DWG NO 0103-00-1115 REV D
CODE IDENT 23338 SHEET 1 OF 3



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TIMING GENERATION
MODE CONTROL
MISC. CONTROL
SWEEP SPEED CONTROL
FREQUENCY RANGE CONTROL
FUNCTION CONTROL
P4
J6
REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN R. BENEDICT
WAVETEK SAN DIEGO • CALIFORNIA
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
0103-00-1115
D
CODE IDENT 23338
SHEET 2

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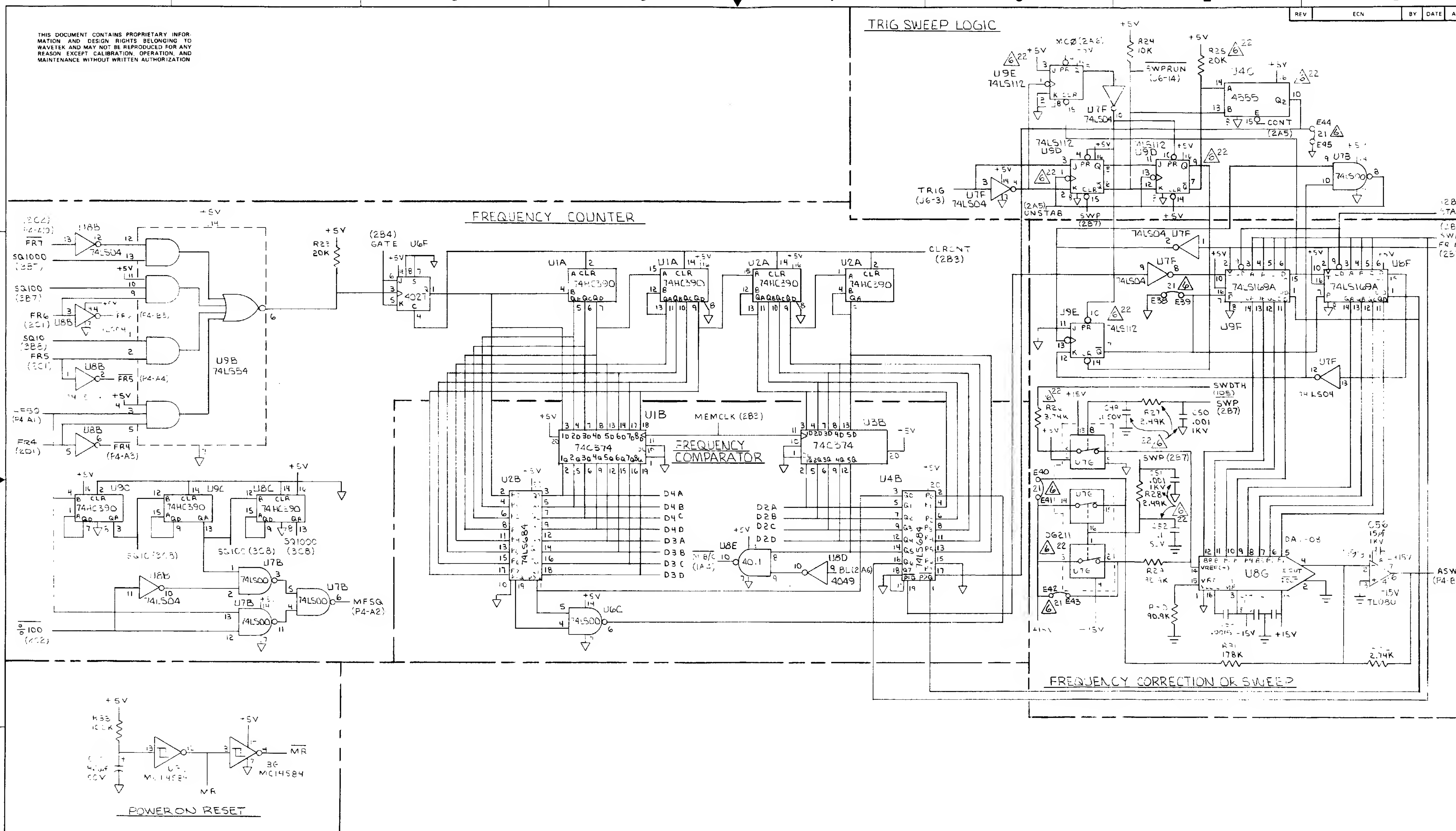

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT
MATERIAL	PROJ ENGR
FINISH WAVETEK PROCESS	RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1	DO NOT SCALE DWG

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC STABILIZER CONTROL BOARD (A3)

MODEL NO 21/22 — DWG NO 0103-00-1115 — REV D

CODE IDENT 23338 — SHEET 3 OF 3

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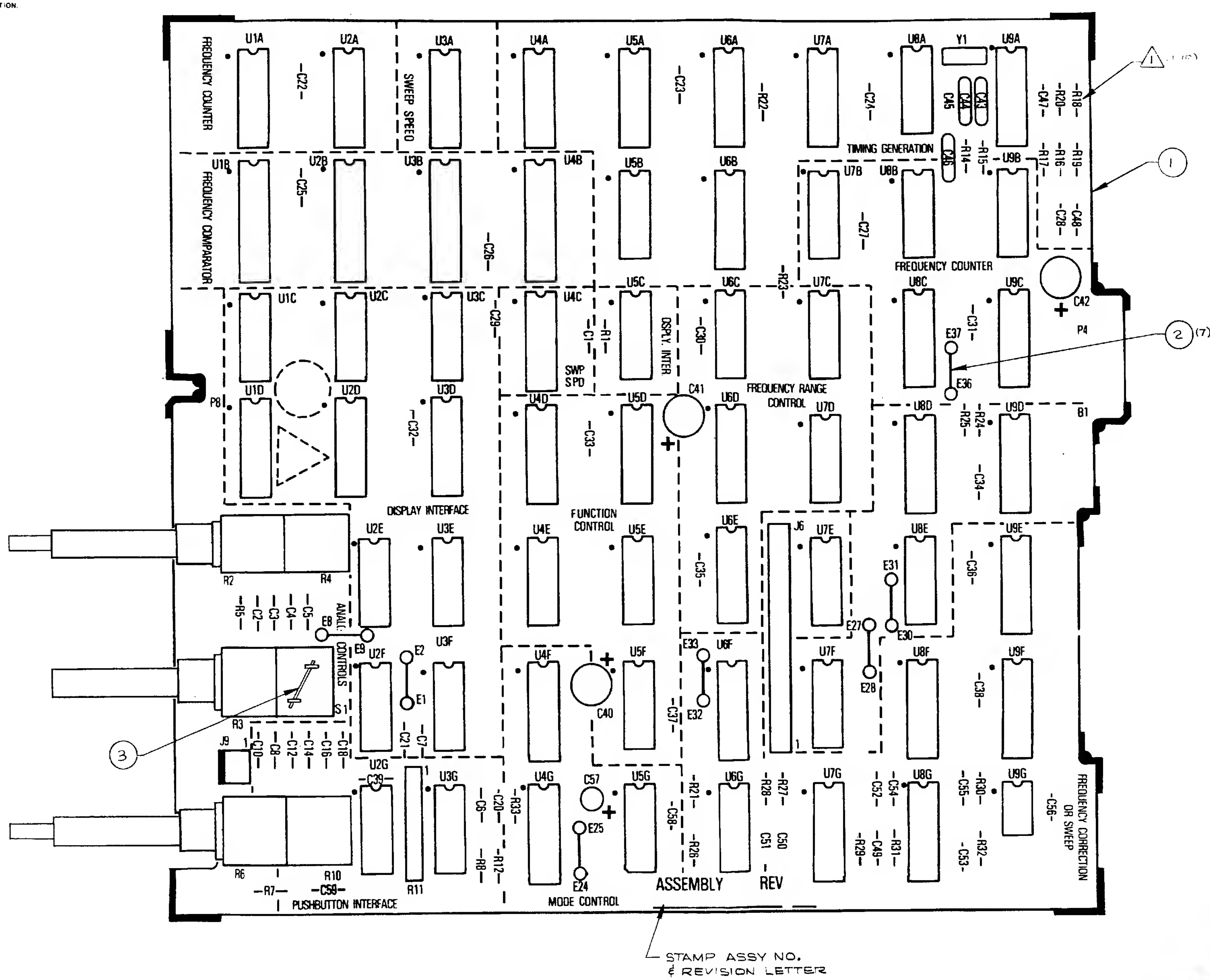
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 4/13/83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE PCA. STAB./ CONTROL (A3)
	RELEASE APPROV	11-15-83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
—	DO NOT SCALE DWG		
	SCALE 2/1	MODEL NO 22	DWG NO 1100-00-1123 F
		CODE IDENT 23338	

1100-00-1123 F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, STAB. /CONT	0103-00-1115	WVTK	0103-00-1115	1
C45T	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C50 C51	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	2
C1 C10 C12 C14 C16 C18 C20 C21 C47 C48 C6 C7 C8	CAP, CER MN .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	13
C2 C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C4 C49 C5 C52 C54 C55 C58 C59	CAP, CER MON, .1MF 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	28
C56	CAP, CE 5PF, [illegible]	DD-150	CRL	1500-01-5011	1
C53	CAP, CER .0015MF 1KV	DD-152 LONG LEAD	CRL	1500-01-5201	1
C44	CAP, MICA, 20PF, 500V	DM15-200J	ARCO	1500-12-0000	1
C46	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	1
C43	CAP, MICA, 75PF, 500V	DM15-750J	ARCO	1500-17-5000	1
C40 C41 C42	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	3
C57	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	1
1	STAB. /CONTROL BD	21-1115	WVTK	1700-00-1115	1

WAVETEK PARTS LIST — TITLE: PCA, STAB. /CONTROL — ASSEMBLY NO: 1100-00-1123 — REV: F — PAGE: 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J9	CONN HEADER 3 PIN	640456-3	AMP	2100-02-0116	1
J6	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0151	1
Y1	CRYSTAL, 6.4MHZ	VF640	VA-FI	2300-99-0015	1
R2, R4	POT, DUAL, 5K	4600-25-0201	WVTK	4600-25-0201	1
R6, R10	POT, DUAL, 5K, 500	4600-25-0202	WVTK	4600-25-0202	1
R3	POT, SWITCH, 5K	4602-05-0303	WVTK	4602-05-0303	1
R14 R17 R21 R24	RES, MF, 1/8W, 1%, 10K	RN550-1002F	TRW	4701-03-1002	4
R33	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R15 R16	RES, MF, 1/8W, 1%, 1.5K	RN550-1501F	TRW	4701-03-1501	2
R31	RES, MF, 1/8W, 1%, 178K	RN550-1783F	TRW	4701-03-1783	1
R22 R23 R25	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R20 R27 R28	RES, MF, 1/8W, 1%, 2.49K	RN550-2491F	TRW	4701-03-2491	3
R32	RES, MF, 1/8W, 1%, 2.74K	RN550-2741F	TRW	4701-03-2741	1
R26	RES, MF, 1/8W, 1%, 3.74K	RN55D-3741F	TRW	4701-03-3741	1
R7	RES, MF, 1.8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	1
R5	RES, MF, 1/8, 1%, 499	RN550-4990F	TRW	4701-03-4990	1
R1 R12 R8	RES, MF, 1/8W, 1%, 499K	RN550-4993F	TRW	4701-03-4993	3

WAVETEK PARTS LIST — TITLE: PCA, STAB. /CONTROL — ASSEMBLY NO. 1100-00-1123 — REV: F — PAGE: 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R18	RES, MF, 1/8W, 1%, 6.04K	RN550-6041F	MEPCO	4701-03-6041	1
R19	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
R29 R30	RES, MF, 1/8W, 1%, 90.9K	RN550-9092F	TRW	4701-03-9092	2
R11	RES MODULE, 470K	810-1-474-J	TRW	4770-00-0034	1
2	RESISTOR, 0 OHM JUMPER	JPW-02A	ROHM	4799-00-0087	7
3	BUSS WIRE, 22GA	298	ALPHA	6000-92-2000	1
4	SLEEVING, 22GA	TFT-200-22	ALPHA	6001-12-2000	1
U8G	IC	DAC-08EQ	AMD	7000-00-0800	1
U9G	IC, OP-AMP	TL080CP	TI	7000-00-8001	1
U9A	IC	CA-3096AE	RCA	7000-30-9600	1
U7G	IC, QUAD SPST CMOS ANALOG SWITCH	DG211CJ	SILX	8000-02-1100	1
U5F U5G U8E	IC	CD4011BE	RCA	8000-40-1100	3
U6F	IC, JK FLIP-FLOP	4027B	NSC	8000-40-2700	1
U1C U2C U2E U2F U3C U3E U3F	IC	CD4030AE	RCA	8000-40-3001	7
U5C	IC, MULTIVIBRATOR	4047B	NSC	8000-40-4700	1
U7E	IC	CD4081BE	RCA	8000-40-8100	1

WAVETEK PARTS LIST — TITLE: PCA, STAB. /CONTROL — ASSEMBLY NO. 1100-00-1123 — REV: F — PAGE: 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U1D U2D U3D	IC, BCD TO LCD	4543B	NSC	8000-45-4300	3
U4C	IC	F4555B	FAIR	8000-45-5500	1
U6C U7B	IC	74LS00	TI	8000-74-0010	2
U7F U8B	IC	74LS04	TI	8000-74-0410	2
U4E U7C U7D	IC, 3 INPUT NAND	74HC10	MOT	8000-74-1040	3
U6D	IC, 1-OF-10 DECODER	74HC42	MOT	8000-74-4240	1
U9B	IC	74LS54	TI	8000-74-5410	1
U6G	IC	MC14012UBCP	MOT	8001-40-1200	1
U8D	IC	CD4049UBE	RCA	8001-40-4900	1
U5E	IC	MC14071B	MOT	8001-40-7100	1
U3A	IC	CD4520BE	RCA	8001-45-2000	1
U4A	IC, 4 INPUT MUX	MC14539	MOT	8001-45-3900	1
U2G U3G	IC, SCHMITT TRIGGER	MC14584B	MOT	8001-45-8400	2
U5B	IC, JK FLIP-FLOP	MM74HC107	NSC	8007-41-0740	1
U9D U9E	IC	74LS112	TI	8007-41-1210	2
U4D U4F	IC, 1 OF 8 DECODER/ DEMULTIPLEXER	74HC138	MOT	8007-41-3840	2
U6B	IC, 2 INPUT MUX	74HC157	MOT	8007-41-5740	1

WAVETEK PARTS LIST — TITLE: PCA, STAB. /CONTROL — ASSEMBLY NO. 1100-00-1123 — REV: F — PAGE: 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8F U9F	IC	SN74LS169BN	TI	8007-41-6911	2
U4G U5D U6E	IC, UP/DOWN COUNTER	MM74HC193	NSC	8007-41-9340	3
U1B U3B	IC	74C374	NAT	8007-43-7430	2
U1A U2A U5A U6A U7A U8C U9C	IC, DECADE COUNTER	MM74HC390	NSC	8007-43-9040	7
U8A	IC, 4-BIT COUNTER	MM74HC393	NSC	8007-43-9340	1
U2B U4B	IC, 8-BIT COMPARATOR	74LS684	TI	8007-46-8410	2

WAVETEK PARTS LIST — TITLE: PCA, STAB. /CONTROL — ASSEMBLY NO. 1100-00-1123 — REV: F — PAGE: 5

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES ·1 XX · 030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST PCA STAB/CONTROL

MODEL NO	DWG NO	REV
22	1100-00-1123	F

CODE IDENT 23338 — SHEET 1 OF 1

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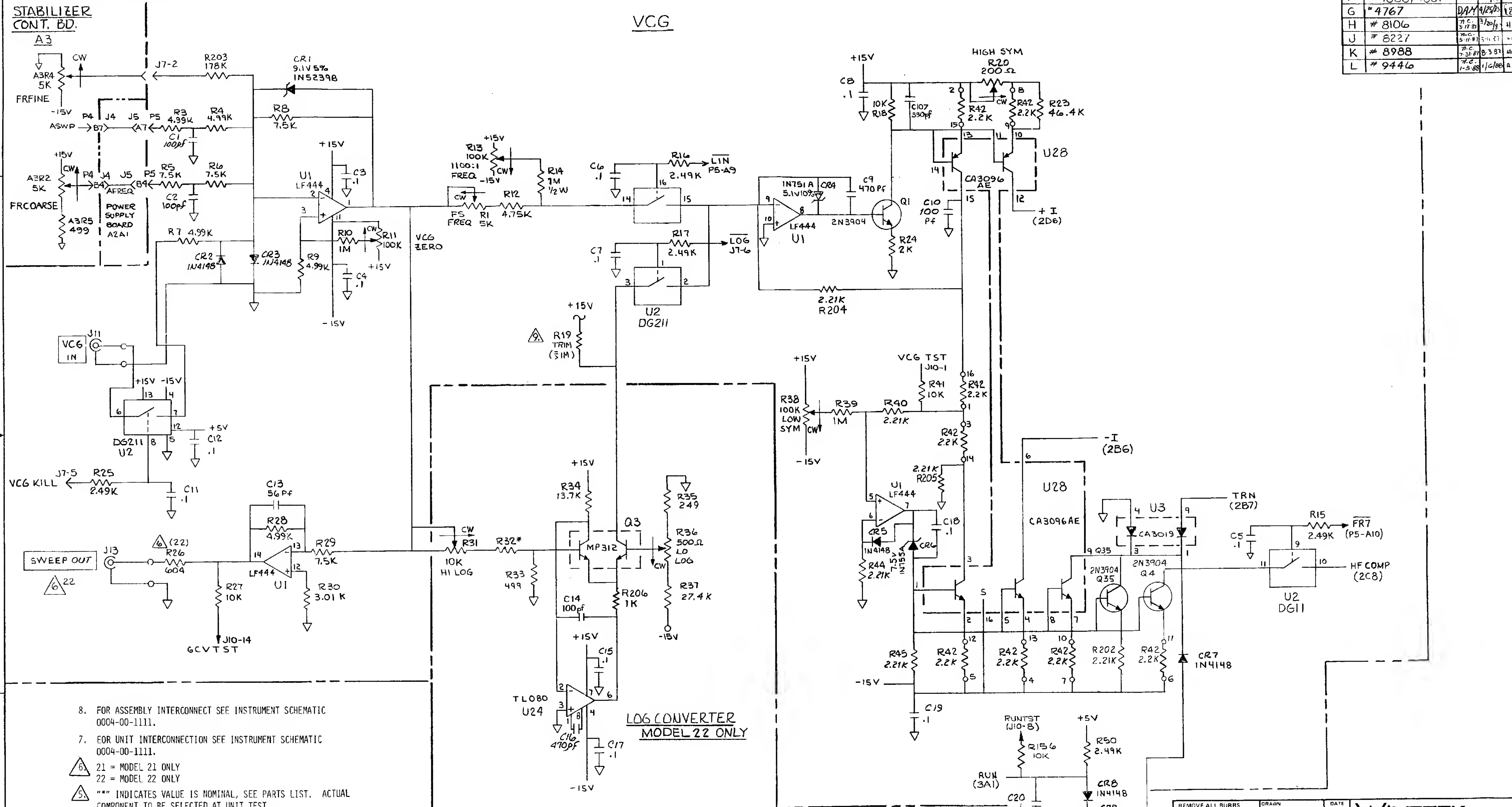
REV	ECN	BY	DATE	APP
C	#4138			
D	#4148			
E	#4194			
F	#4388/4601	KA		
G	#4767	DAM		
H	#8106			HN
J	#8227			
K	#8988			
L	#9446			A R.T.



8. FOR ASSEMBLY INTERCONNECT SEE INSTRUMENT SCHEMATIC 0004-00-1111.
7. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
6. 21 = MODEL 21 ONLY
22 = MODEL 22 ONLY
5. "*" INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
4. CAPACITOR VALUES ARE IN MICROFARADS (uf).
3. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.
2. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A4.
1. TRANSISTORS HAVE 2800-11-0001 HEATSINK AND 2800-11-0017 TRANSIPAD.

9. "TRIM" INDICATES VALUE SELECTED AT UNIT CALIBRATION.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN R. BENEDICT | WAVETEK SAN DIEGO · CALIFORNIA

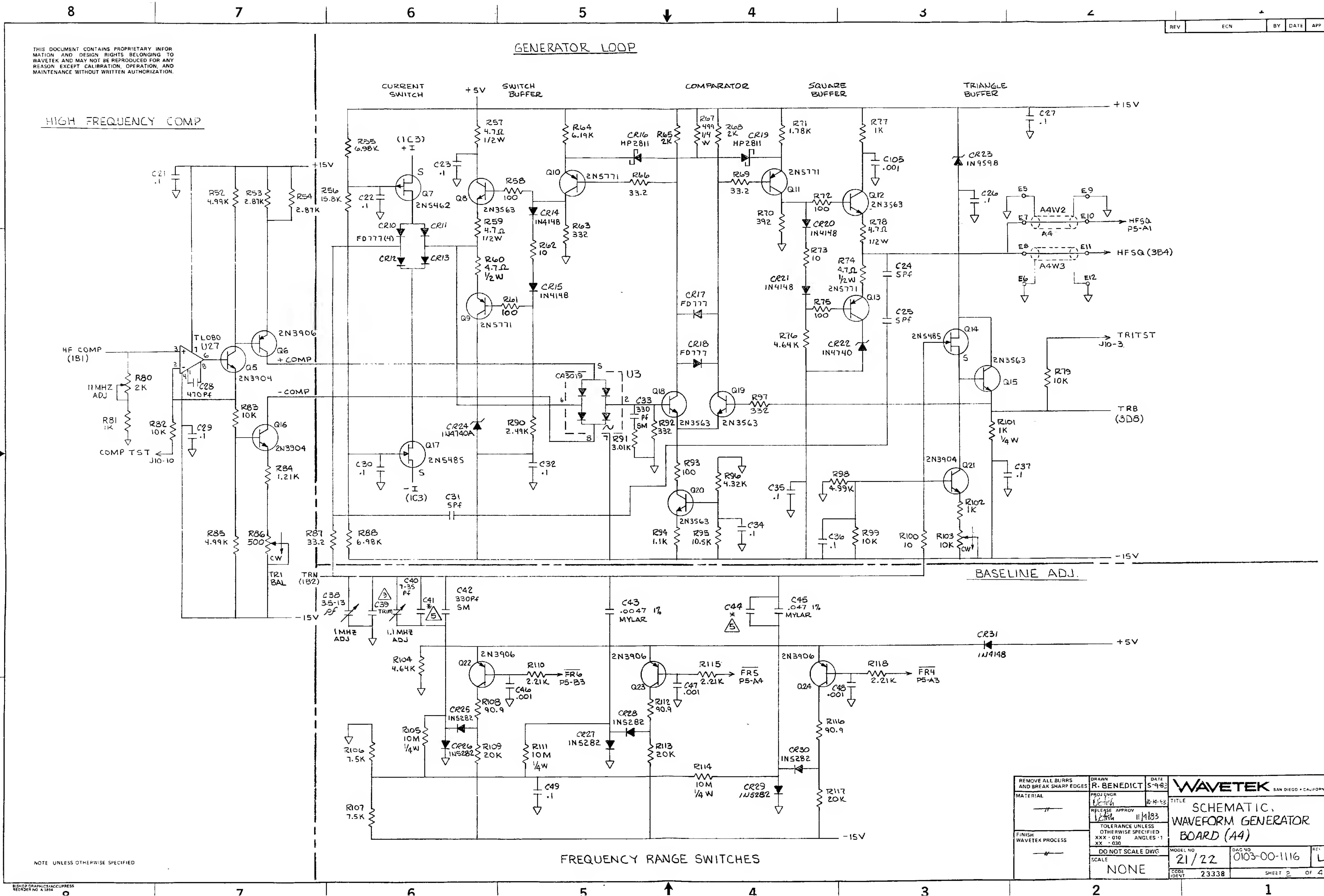
MATERIAL | TITLE: SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)

FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030

DO NOT SCALE DWG | SCALE NONE | MODEL NO 21/22 | DWG NO 0103-00-1116 | REV L

CODE IDENT 23338 | SHEET 1 OF 4

0103-00-1116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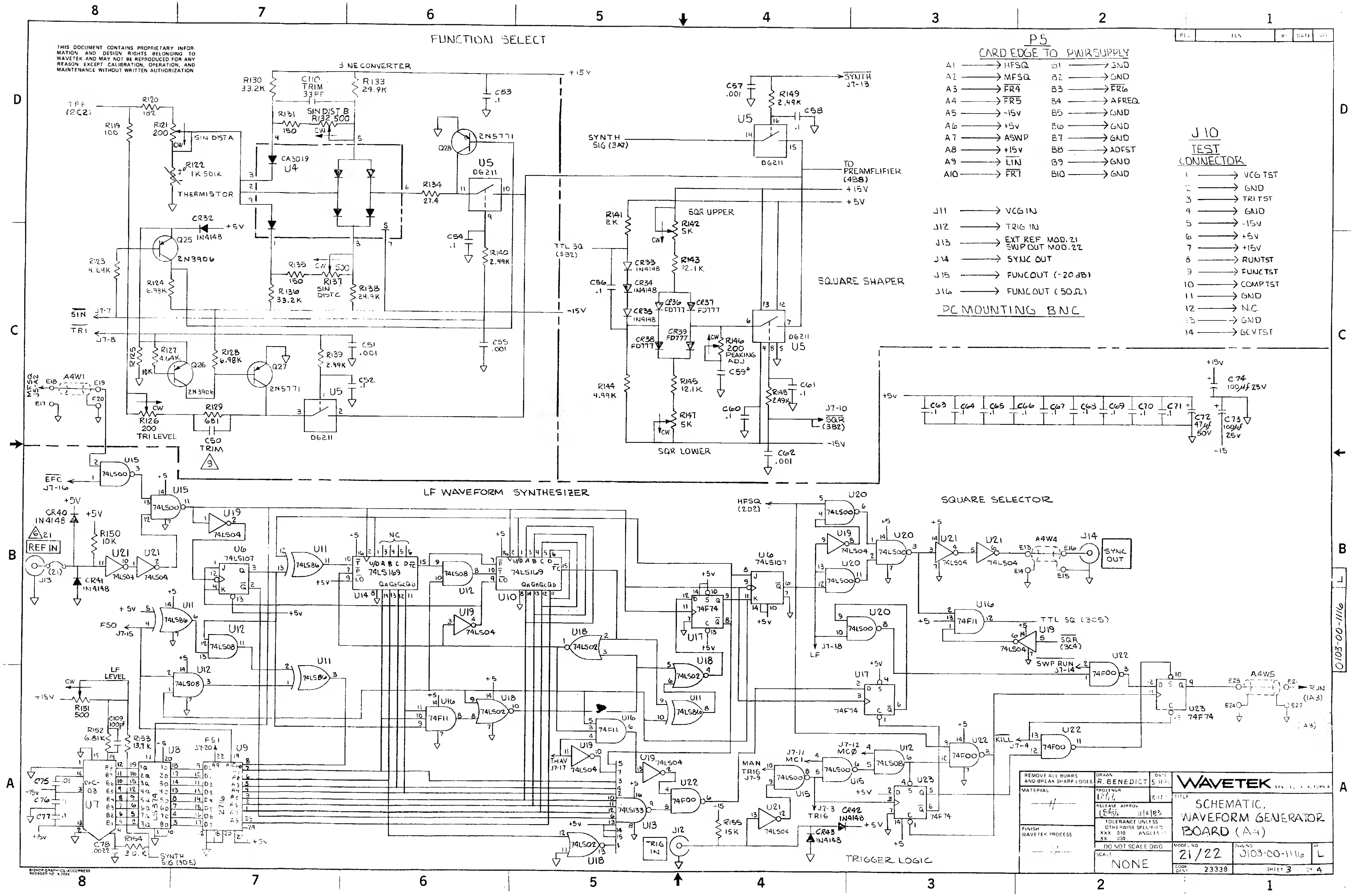
HIGH FREQUENCY COMP
GENERATOR LOOP
CURRENT SWITCH
SWITCH BUFFER
COMPARATOR
SQUARE BUFFER
TRIANGLE BUFFER
BASELINE ADJ.
FREQUENCY RANGE SWITCHES
HF COMP (1B1)
COMP TST J10-10
TRITST J10-3
TRB (3D8)
HFSQ P5-A1
HFSQ (3B4)
TR1 BAL
TRN (1B2)
1 MHZ ADJ
1.1 MHZ ADJ
11 MHZ ADJ
FR6 P5-B3
FR5 P5-A4
FR4 P5-A3
+15V
-15V
+5V
NOTE UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN R. BENEDICT
DATE 5-9-83
RELEASE APPROV 11/4/83
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
MODEL NO 21/22
DWG NO 0103-00-1116
REV L
CODE IDENT 23338
SHEET 2 OF 4
0103-00-1116



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FUNCTION SELECT
SINE CONVERTER
SQUARE SHAPER
LF WAVEFORM SYNTHESIZER
SQUARE SELECTOR
TRIGGER LOGIC
P5
CARD EDGE TO PWR SUPPLY
A1 → HFSQ
A2 → MFSQ
A3 → FR4
A4 → FR5
A5 → -15V
A6 → +5V
A7 → ASWP
A8 → +15V
A9 → LIN
A10 → FRT
B1 → GND
B2 → GND
B3 → FR6
B4 → AFREQ
B5 → GND
B6 → GND
B7 → GND
B8 → AOFST
B9 → GND
B10 → GND
J11 → VCG IN
J12 → TRIG IN
J13 → EXT REF MOD. 21 SWP OUT MOD. 22
J14 → SYNC OUT
J15 → FUNC OUT (-20dB)
J16 → FUNC OUT (50Ω)
PC MOUNTING BNC
J10
TEST CONNECTOR
1 → VCG TST
2 → GND
3 → TRI TST
4 → GND
5 → -15V
6 → +5V
7 → +15V
8 → RUN TST
9 → FUNC TST
10 → COMP TST
11 → GND
12 → N.C.
13 → GND
14 → GCV TST
REF IN
SYNC OUT
TRIG IN
SYNTH SIG (3A7)
TO PREAMPLIFIER (4B8)
THERMISTOR
TRI LEVEL
SIN DIST A
SQR UPPER
SQR LOWER
LF LEVEL
REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN R. BENEDICT
WAVETEK
SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
DO NOT SCALE DWG
SCALE NONE
21/22
0103-00-1116
L
23338
SHEET 3 OF 4
0103-00-1116
BISHOP GRAPHICS/ACCUPRESS

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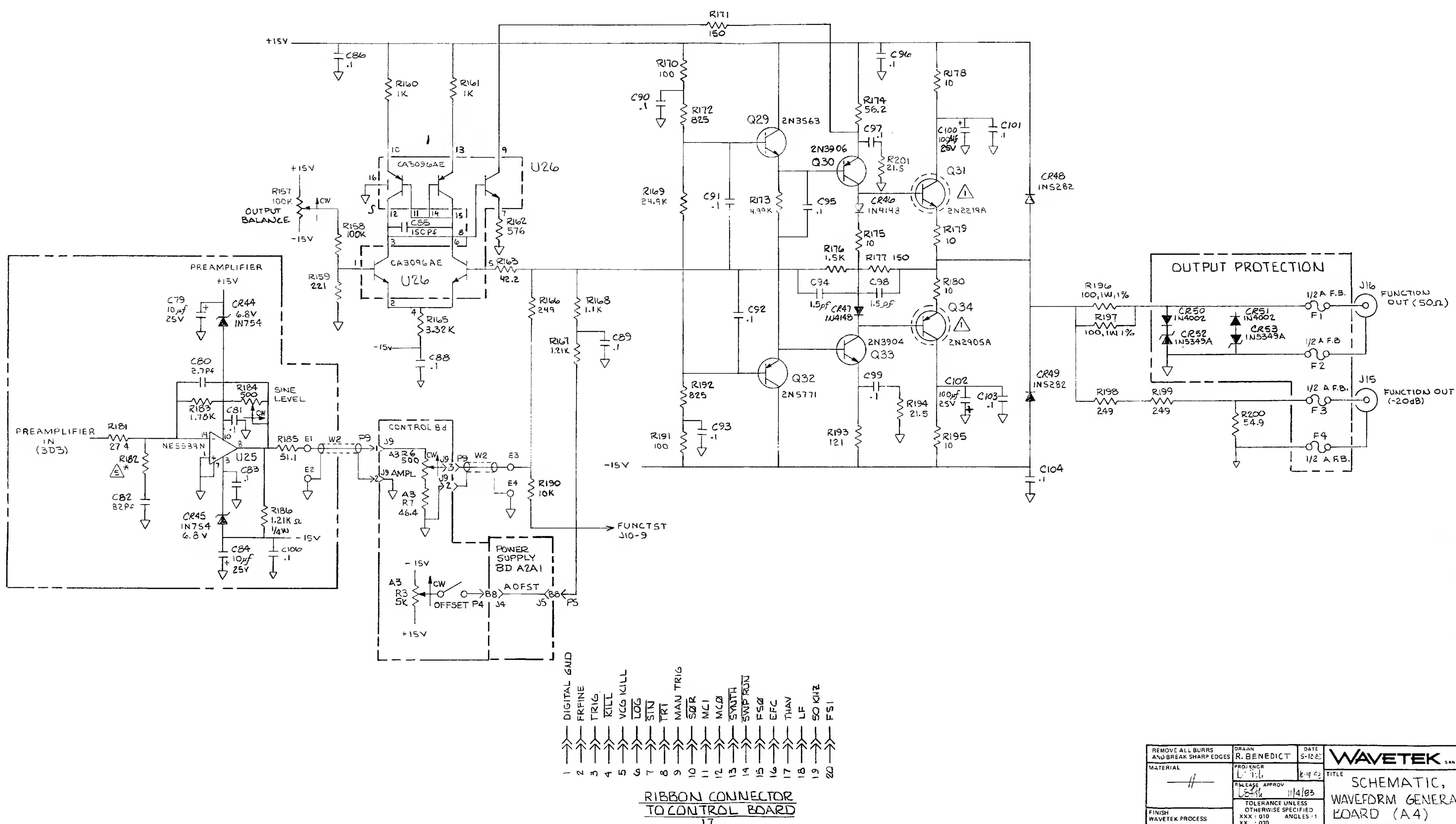
REV	ECN	BY	DATE	APP

OUTPUT AMPLIFIER



RIBBON CONNECTOR TO CONTROL BOARD J7

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-12-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
	RELEASE APPROV	11/4/83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: .010 ANGLES ±1 XX: .030		
—	DO NOT SCALE DWG		MODEL NO 21/22 — DWG NO 0103-00-1116 — REV L
	SCALE NONE		CODE IDENT 23338 — SHEET 4 OF 4

0103-00-1116 L

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3054

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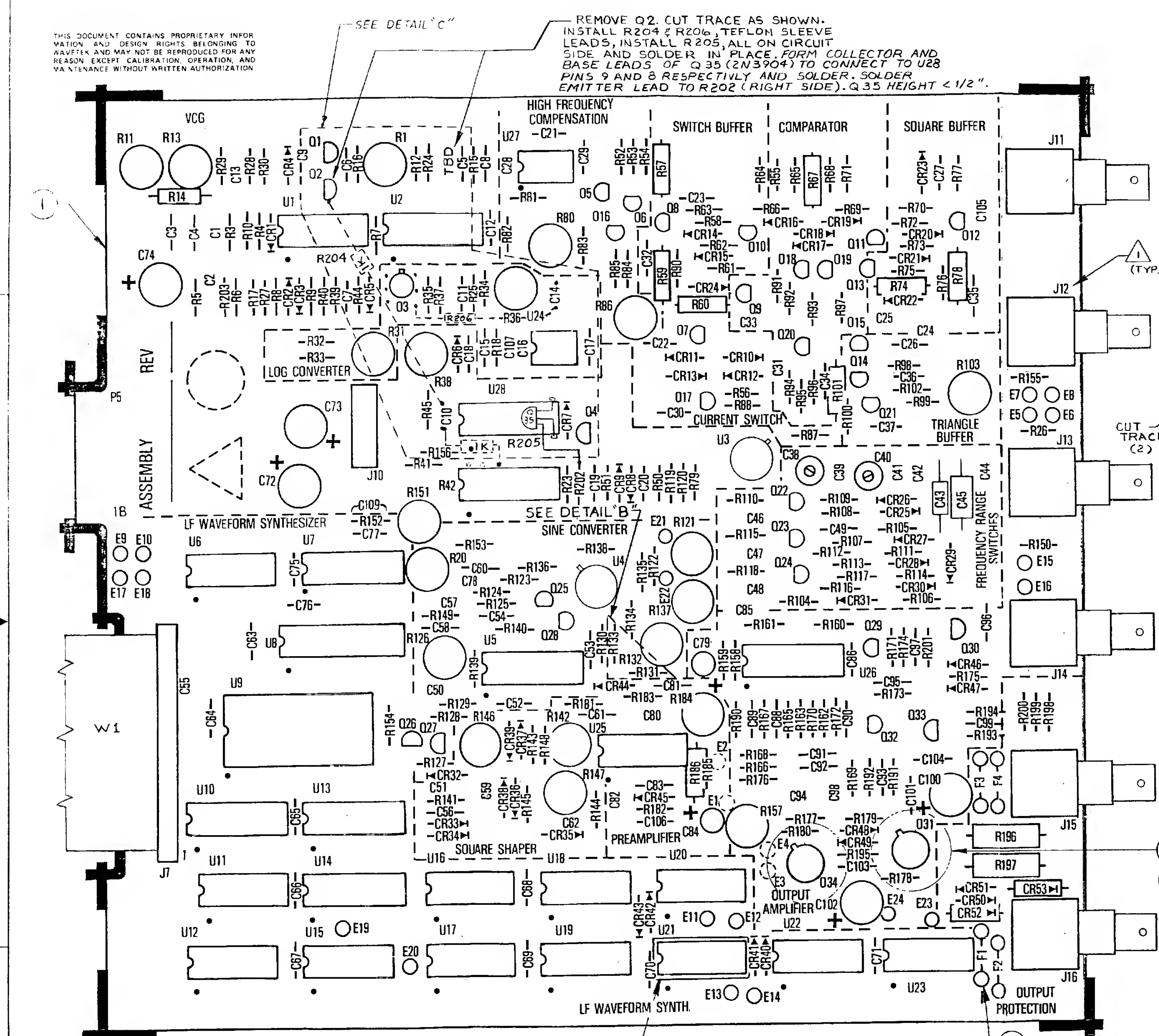
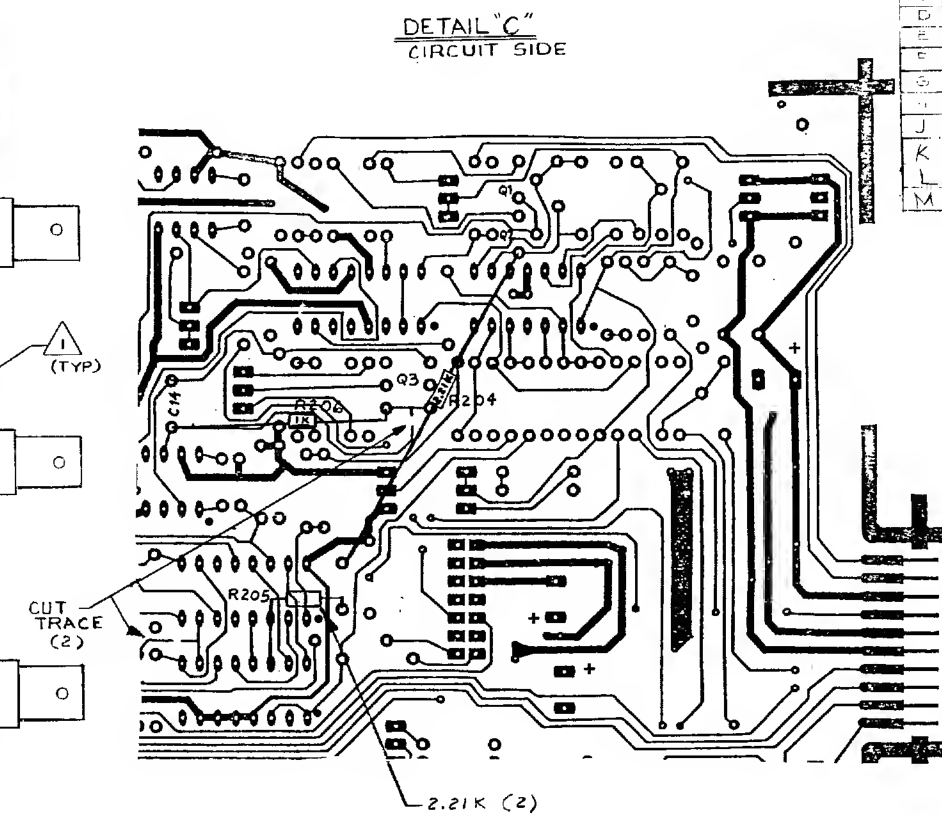
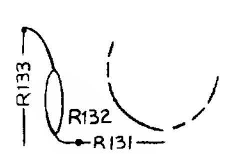
REV	ECN	BY	DATE	APP
[illegible]	4037	A.T.	[illegible]	
[illegible]	4148	A.T.	[illegible]	
D	4194	A.T.	[illegible]	
E	4727	M.F.	4-25-[illegible]	
F	4767	D.M.	4-25-[illegible]	
G	8106	[illegible]	3-20-87	HN
H	8227	[illegible]	5-11-87	HN
J	8988	[illegible]	[illegible]	HN
K	944[illegible]	[illegible]	[illegible]/88	[illegible]
L	89-134 BOM	BG	7-27-89	KK
M	89-335 BOM	BG	7-27-89	KA







DETAIL "B"

CABLE HOOKUP LIST					
REF DES	DESTINATION FROM	DESTINATION TO	REF DES	DESTINATION FROM	DESTINATION TO
A4 W1	E18	E19	A4 W5	E21	E23
	E17 ⏚	E20 ⏚		E22 ⏚	E24 ⏚
A4 W2	E10	E7	W2	P9-1	E1
	E9 ⏚	E5 ⏚		P9-2 ⏚	E2 ⏚
A4 W3	E8	E11		P9-3	E3
	E6 ⏚	E12 ⏚		P9-2 ⏚	E4 ⏚
A4 W4	E16	E13			
	E15 ⏚	E14 ⏚			

6. WIRES AND CABLES OBTAINED FROM CABLE KIT 1207-00-1120.
5. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
4. C39 & C50 VALUES ARE TO BE SELECTED & INSTALLED AT UNIT TEST.
3. C41 VALUE IS NOMINAL. ACTUAL COMPONENT VALUES TO BE SELECTED AT UNIT TEST.
2. SEE 0103-00-1116 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A4.

NOTES:

SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 6/26/8[illegible]	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL —	PROJ ENGR [illegible]		TITLE PCA, WAVEFORM GENERATOR (A4)	
	RELEASE, APPROV [illegible]	[illegible]-15-83		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°			
	DO NOT SCALE DWG		MODEL NO 22	DWG NO 1100-00-1124 REV M
	SCALE 2/1		CODE IDENT 23338	SHEET 1 OF 2

1100-00-1124 M

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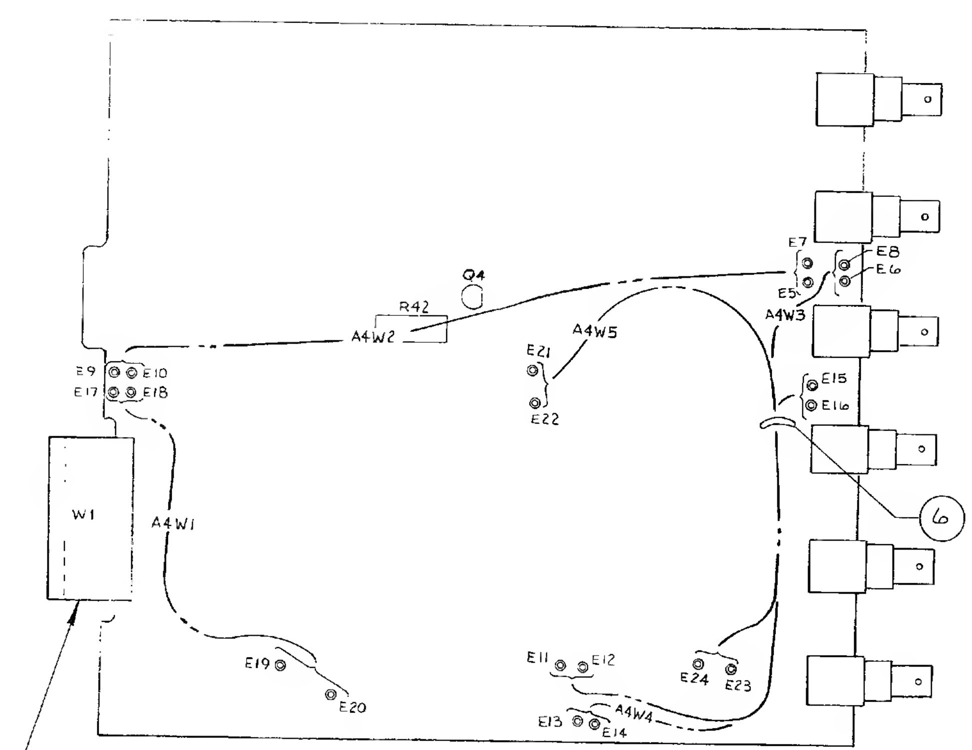
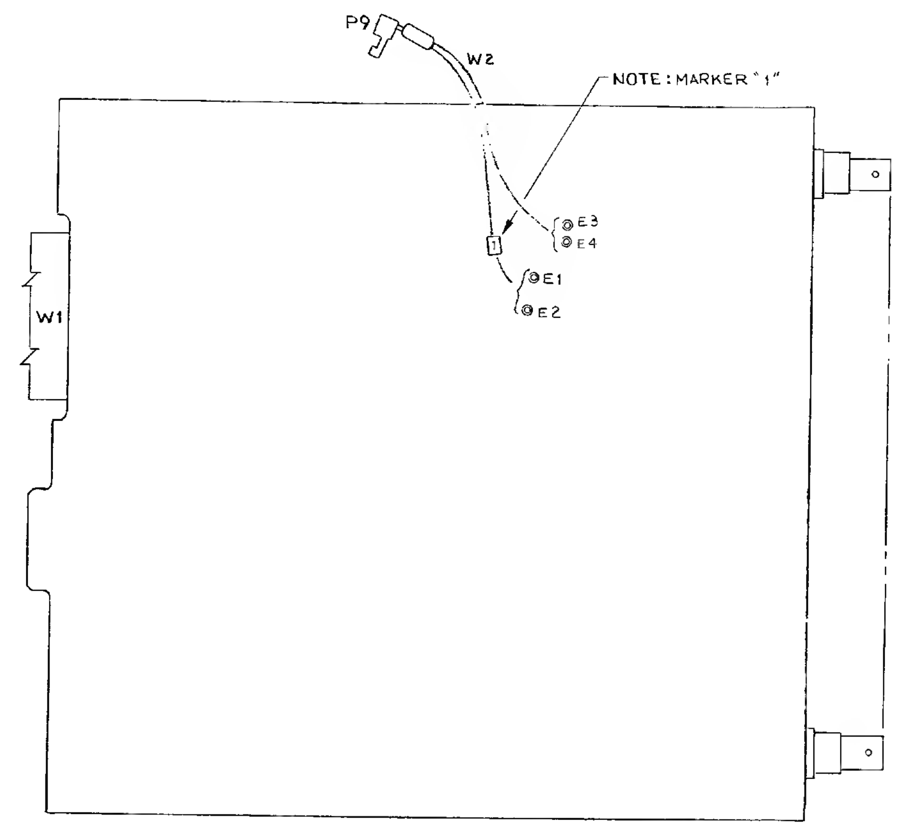
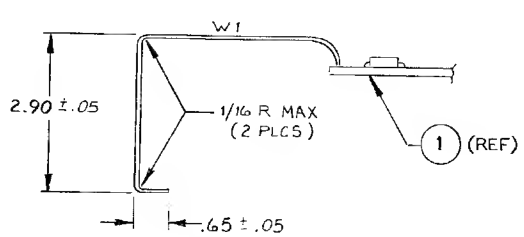
REV	ECO	BY	DATE	APP
SEE SHT 1 FOR REVISIONS				



CABLE INSTALLATION
(COMPONENT SIDE)
SCALE: 1/1



CABLE INSTALLATION
(SOLDER SIDE)
SCALE: 1/1



DETAIL "A"
CABLE FORMING / INSTALLATION

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 7-30-87
MATERIAL —	CHECKED NGUYEN HIEU	8-6-87
	PROJ ENGR.	8/6/87
	RELEASE APPROV.	8/18/87
FINISH WAVETEK PROCESS —	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± 1/64 DECIMALS .XX ± .030 .XXX ± .010 ANGLES ± 1°	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PCA, WAVEFORM GENERATOR (A4)

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-1124	M

SCALE NOTED | MODEL 22 | SHEET 2 OF 2

1100-00-1124 M

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, WAVE/GEN	0103-00-1116	WVTK	0103-00-1116	1
R42	RES, NETWORK, 2 2K OHM 1% X8	4116R-001-2.2K	BOURN	128 2223	1
C24 C25 C31	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	3
C1 C10 C109 C14 C2	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	5
C105 C44T C46 C47 C48 C51 C55 C57 C62	CAP, CER, .001UF, 1KV	DD-102	CRL	1500-01-0211	9
C75	CAP CER MON 01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C101 C103 C104 C106 C11 C12 C15 C17 C18 C19 C20 C21 C22 C23 C26 C27 C29 C3 C30 C32 C34 C35 C36 C37 C4 C49 C5 C52 C53 C54 C56 C58 C6 C60 C61 C63 C64 C65 C66 C67 C68 C69 C7 C70 C71 C76 C77 C8 C81 C83 C86 C88 C89 C90 C91 C92 C93 C95 C96 C97 C99	CAP, CER, MON, 1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	61
C85	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1
C94 C98	CAP, CER, 1.5PF, 1KV	NCD1.5PF1KVK750-CR	NIC	1500-01-5507	2
C78	CAP, CER, .0022, 1KV	DD-222SLL	CRL	1500-02-2201	1
C80	CAP CER MON 2 7PF 50V	CCD2R7DNPO	ARCO	1500-02-7505	1

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C110T	CAP, CER, 33PF, 1KV	DD-330 LONG LEAD	CRL	1500-03-3001	1
C59T	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C107	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C16 C28 C9	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	3
C13	CAP, CER, 56PF, 1KV	DD-560	CRL	1500-05-6001	1
C82	CAP, CER, 82PF, 1KV	DD-820	CRL	1500-08-2011	1
C33 C42	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C41T	CAP, MICA, 82PF, 500V	DM15-820J	ARCO	1500-18-2000	1
C79 C84	CAP, ELECT, 10MF/25V RADIAL LEAD, SP 10	NRE 10/63	NIC	1500-31-0002	2
C100 C102 C73 C74	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP 20	NRE101M35V8X11	NIC	1500-31-0102	4
C72	CAP, ELECT, 47MF, 50V RADIAL LEAD, SP 20	UL81J470M	NICH	1500-34-7003	1
C38	CAP, VAR, 3 5-13PF, 250V	7S-TRIKO-02 3 5/13PF	TRIKO	1500-51-3000	1
C40	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	1
C45	CAP, MET POLY, 047MFD, 50V, +-1% AXIAL	C31A473F	BISHO	1509-90-0062	1

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C43	CAP, MET POLY, .0047MFD, 50V, +-1 % AXIAL	C31A472F	BISHO	1509-90-0063	1
1	WAVEFORM GEN BD	21-1116	WVTK	1700-00-1116	1
J11 J12 J13 J14 J15 J16	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	6
2	SKT, IC, 14 PIN	DILB14P-108T	BURND	2100-03-0066	1
3	SOCKET, MINISERT	75060-012	BERG	2100-03-0076	8
J10	CONN, HEADER, 14 PIN 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
F1 F2 F3 F4	FUSE, 1/2A, 125V(PC)	255.500	LITFU	2400-05-0035	4
4	HEAT SINK	207	WAKE	2800-11-0001	2
5	TRANSIPAD	333-125-NY	BLINN	2800-11-0017	2
6	MOUSETAIL	2829-75-2	RUBTK	2800-12-0005	1
R11 R13 R157 R38	POT, TOP TRIM, 20T, 100K	68WR100K	BECK	4609-90-0001	4
R103 R31	POT, TOP TRIM, 20T, 10K	68WR10K	BECK	4609-90-0002	2
R80	POT, TOP TRIM, 20T, 2K	68WR2K	BECK	4609-90-0004	1
R1 R142 R147	POT, TOP TRIM, 20T, 5K	68WR5K	BECK	4609-90-0013	3
R121 R126 R146 R20	POT, TOP TRIM, 20T, 200	68WR200	BECK	4609-90-0020	4

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R132 R137 R151 R184 R36 R86	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	6
R57 R59 R60 R74 R78	RES, C, 1/2W, 5%, 4 7	RC-1/2-4R7J	STKPL	4700-25-0479	5
R14	RES, C, 1/2W, 5%, 1M	RC-1/2-105J	STKPL	4700-25-1004	1
R119 R170 R191 R58 R61 R72 R75 R93	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	8
R102 R160 R161 R206 R77 R81	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	6
R125 R150 R156 R18 R190 R27 R41 R79 R82 R83 R99	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	11
R158	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R10 R39	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	2
R100 R175 R178 R179 R180 R195 R62 R73	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	8
R95	RES, MF, 1/8W, 1%, 10 5K	RN55D-1052F	TRW	4701-03-1052	1
R168 R94	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	2
R193	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701-03-1210	1
R167 R84	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	2
R143 R145	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	2

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R153 R34	RES, MF, 1/8W, 1%, 13.7K	RN55D-1372F	TRW	4701-03-1372	2
R131 R135 R171 R177	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	4
R176	RES, MF, 1/8W, 1%, 1 5K	RN55D-1501F	TRW	4701-03-1501	1
R155	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R56	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R183 R71	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R203	RES, MF, 1/8W, 1%, 178K	RN55D-1783F	TRW	4701-03-1783	1
R120	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R141 R24 R65 R68	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	4
R109 R113 R117	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R194 R201	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R159	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	1
R110 R115 R118 R202 R204 R205 R40 R44 R45	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	9
R166 R198 R199 R35	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	4
R139 R140 R148 R149 R15 R16 R17 R25 R50 R90	RES, MF, 1/8W, 1%, 2 49K	RN55D-2491F	TRW	4701-03-2491	10
R133 R138 R169 R32T	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	4

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R37	RES, MF, 1/8W, 1%, 27 4K	RN55D-2742F	TRW	4701-03-2742	1
R134 R181	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	2
R53 R54	RES, MF, 1/8W, 1%, 2 87K	RN55D-2871F	TRW	4701-03-2871	2
R154 R30 R91	RES, MF, 1/8W, 1%, 3 01K	RN55D-3011F	TRW	4701-03-3011	3
R63 R92 R97	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R165	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R130 R136	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R66 R69 R87	RES, MF, 1/8W, 1%, 33 2	RN55D-33R2F	TRW	4701-03-3329	3
R70	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R163	RES, MF, 1/8W, 1%, 42 2	RN55D-42R2F	TRW	4701-03-4229	1
R96	RES, MF, 1/8W, 1%, 4 32K	RN55D-4321F	TRW	4701-03-4321	1
R104 R123 R127 R76	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	4
R23	RES, MF, 1/8W, 1%, 46.4K	RN55D-4642F	TRW	4701-03-4642	1
R12	RES, MF, 1/8W, 1%, 4 75K	RN55D-4751F	TRW	4701-03-4751	1
R33	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R144 R173 R28 R3 R4 R52 R7 R85 R9 R98	RES, MF, 1/8W, 1%, 4 99K	RN55D-[illegible]1F	TRW	4701-03-4991	10

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MODEL 22 PCA WAVEFORM GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
	DO NOT SCALE DWG		MODEL NO / DWG NO 1100-00-1124 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 2

NOTE UNLESS OTHERWISE SPECIFIED

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R182T R185	RES. MF, 1/8W, 1%, 51. 1	RN55D-51R1F	TRW	4701-03-5119	2
R200	RES. MF, 1/8W, 1%, 54 9	RN55D-54R9F	TRW	4701-03-5499	1
R174	RES. MF, 1/8W, 1%, 56 2	RN55D-56R2F	TRW	4701-03-5629	1
R162	RES. MF 1/8W, 1%, 576	RN55D-5760F	TRW	4701-03-5760	1
R26	RES. MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	1
R64	RES, MF, 1/8W, 1%, 6 19K	RN55D-6191F	TRW	4701-03-6191	1
R129	RES. MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R152	RES, MF, 1/8W, 1%, 6 81K	RN55D-6811F	TRW	4701-03-6811	1
R124 R128 R55 R88	RES, MF, 1/8W, 1%, 6. 98K	RN55D-6981F	TRW	4701-03-6981	4
R106 R107 R29 R5 R6 R8	RES, MF, 1/8W, 1%, 7 5K	RN55D-7501F	TRW	4701-03-7501	6
R172 R192	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	2
R51	RES, MF, 1/8W, 1%, 8 25K	RN55D-8251F	TRW	4701-03-8251	1
R108 R112 R116	RES. MF. 1/8W, 1%, 90. 9	RN55D-90R9F	TRW	4701-03-9099	3
R101	RES, MF, 1/4W, 1%, 1K	RN60D1001F	TRW	4701-13-1001	1
R186	RES, MF, 1/4W, 1%, 1 21K	RN60D-1211F	TRW	4701-13-1211	1
R67	RES. MF, 1/4W, 1%, 499	RN60D4990F	TRW	4701-13-4990	1

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R196 R197	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
R105 R111 R114	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	3
CR4	DIODE, ZENER, 5. 1V, 5% TOL, 500MW, G/B, IN751A	1N751A	FAIR	4801-01-0751	1
CR44 CR45	DIODE, ZENER, 6. 8V	1N754A	MOT	4801-01-0754	2
CR6	DIODE, ZENER, 7. 5V, IN755	1N755A	MOT	4801-01-0755	1
CR23	DIODE, ZENER 500MW SILICON PLANAR	1N959	SIEM	4801-01-0959	1
CR22 CR24	DIODE, ZENER 10V, GLASS SILICON, 1W	1N4740A	MOT	4801-01-4740	2
CR1	DIODE, ZENER 9. 1V, GLASS SILICON, 500MW	1N5239	TEL	4801-01-5239	1
CR25 CR26 CR27 CR28 CR29 CR30 CR48 CR49	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	8
CR52 CR53	DIODE, ZENER 12V, SILICON OXIDE, 5W	1N5349A	MOT	4801-01-5349	2
CR50 CR51	DIODE, 1N4002 GEN PURPOSE RECT 100V, 1A	1N4002	FAIR	4801-02-0001	2
CR10 CR11 CR12 CR13 CR17	OIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	10

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR18 CR36 CR37 CR39 DR38 CR14 CR15 CR2 CR20 CR21 CR3 CR31 CR32 CR33 CR34 CR35 CR40 CR41 CR42 CR43 CR46 CR47 CR5 CR/ CR8 CR9	DIODE 1N4148 COMPUTER, G/P, 75V, 200M A, SWITCHING	1N4148	FAIR	4807-02-6666	21
CR16 CR19	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
Q31	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	1
Q34	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	1
Q12 Q15 Q18 Q19 Q20 Q29 Q8	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	7
Q1 Q16 Q21 Q33 Q35 Q4 Q5	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	7
Q22 Q23 Q24 Q25 Q26 Q30 Q6	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906	FAIR	4901-03-9060	7
Q7	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	1
Q14 Q17	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	2
Q10 Q11 Q13 Q27 Q28 Q32 Q9	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	7
R122	THERMISTER	1K-501-K	MC1	5300-00-0011	1

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 9

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
W1	CABLE, FLEX CIRCUIT	1-86947-9	AMP	6001-60-0005	1
U7	DAC, 8BIT HI-SPEED MULT	DAC-08EQ	AMD	7000-00-0800	1
U1	OP AMP, ENHANCED JFET, PRECISION QUAD	TL054CN	TI	7000-0D-5400	1
U24 U27	OP AMP	TL080CP	T1	7000-00-8001	2
Q3	IC	LS312-52	LINSY	7000-08-1200	1
U3 U4	DIODE, ULTRA FAST, LOW CAPACITANCE	CA-3019	RCA	7000-30-1900	2
U26 U28	TRANS ARRAY, NPN/PNP	CA-3096AE	RCA	7000-30-9600	2
U25	OP AMP	NE5539	SIG	7000-55-3900	1
U2 U5	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	2
U22	GATE, NAND, QUAD 21NP, TTL	74F00PC	FAIR	8000-74-0002	1
U15 U20	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	2
U18	GATE, NOR, QUAD, 21NP, TTL	74LS02	TI	8000-74-0210	1
U19 U21	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	2

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U12	GATE AND, QUAD 2-INP, TTL	74LS08	T1	8000-74-0810	1
U16	GATE AND, 3-INP, TTL	74F11PC	FAIR	8000-74-1102	1
U17 U23	FL1P-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	2
U11	GATE XOR, QUAD 21NP, TTL	74LS86	TI	8000-74-8610	1
U6	FL1P-FLOP, DUAL J-K, TTL	74LS107A	TI	8007-41-0710	1
U13	GATE, NAND, 13 INP, TTL	74LS133	FAIR	8007-41-3310	1
U10 U14	COUNTER, SYNC 4 UP-DN, TTL	SN74LS169BN	TI	8007-41-6911	2
U8	FL1P-FLOP, OCT D, TTL	74LS374	T1	8007-43-7410	1
U9	IC, PROGRAMMED REF; 8000-27-1600	8600-00-0249	WVTK	8600-00-0249	1

WAVETEK PARTS LIST — TITLE: PCA, WAVEFORM GEN — ASSEMBLY NO. 1100-00-1124 — REV M — PAGE 11

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA WAVEFORM GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES · 1 XX :.030		
	DO NOT SCALE DWG		MODEL NO 22 — DWG NO 1100-00-1124 — REV
	SCALE		CODE IDENT 23338 — SHEET 2 OF 2

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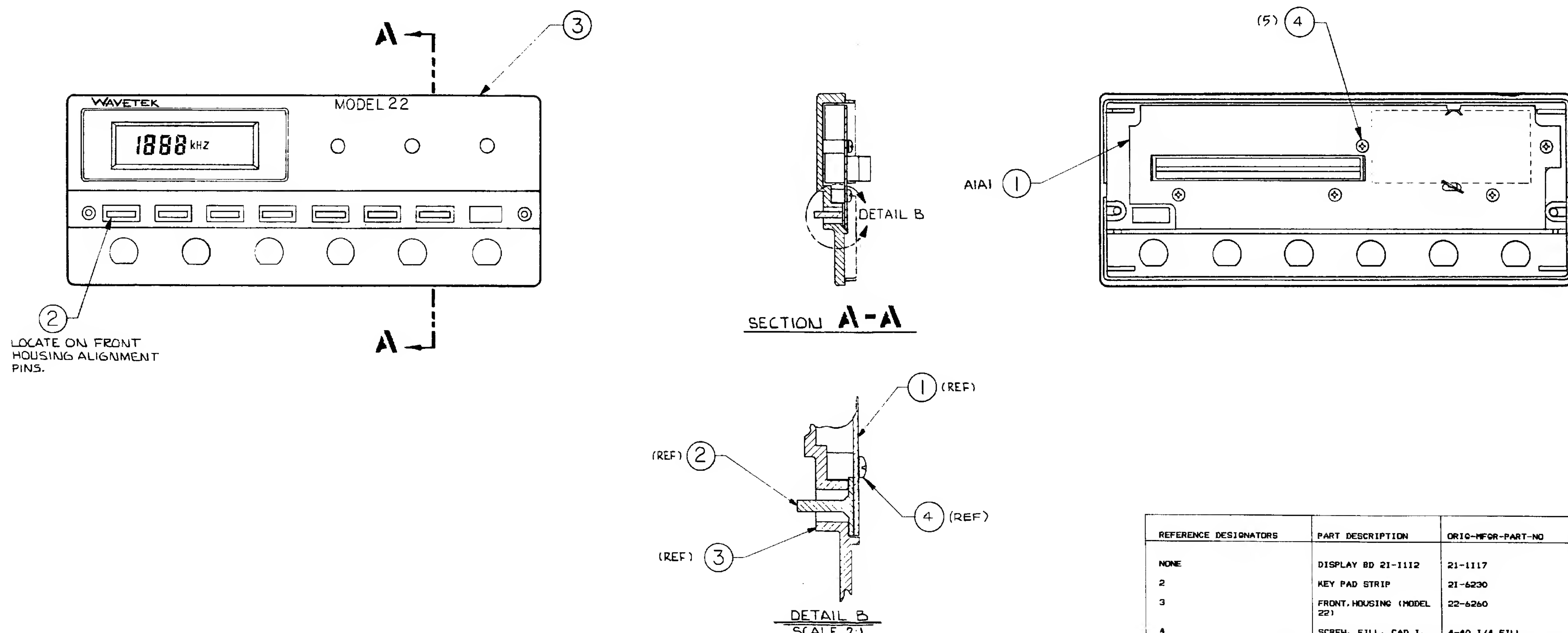
REV	ECN	BY	DATE	APP
A	[illegible]		[illegible]	



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	DISPLAY BD 21-1112	21-1117	WVTK	1208-00-1117	1
2	KEY PAD STRIP	21-6230	WVTK	1400-01-6230	1
3	FRONT, HOUSING (MODEL 22)	22-6260	WVTK	1400-01-6260	1
4	SCREW, FILL, CAD I, CROSS RECESS, 4-40 X 1/4	4-40 1/4 FILL	CMRCL	2800-39-4104	5

1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 1204-21-1111.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.MAGNOLIA	DATE 6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY FRONT PANEL MODEL 22 (A1)
	RELEASE APPROV	11-15-83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
	DO NOT SCALE DWG		MODEL NO 22 / DWG NO 1101-00-1122 / REV A
	SCALE FULL		CODE IDENT 23338 / SHEET 1 OF 1

1101-00-1122 A

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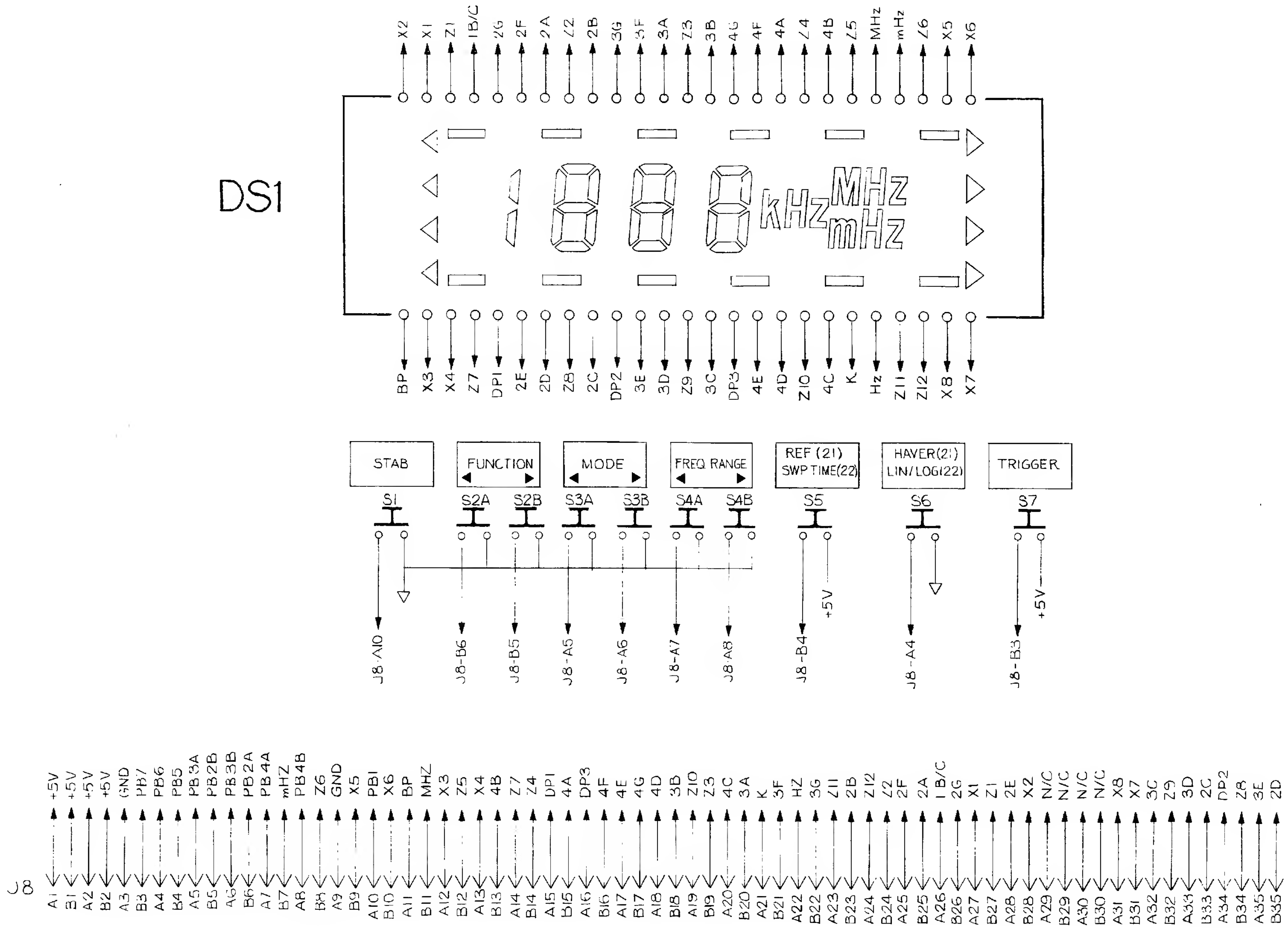

2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1A1.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1°

DO NOT SCALE DWG

SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, DISPLAY (A1A1)

MODEL NO 21/22

DWG NO 0103-00-1117

CODE IDENT 23338

SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
A	7728			

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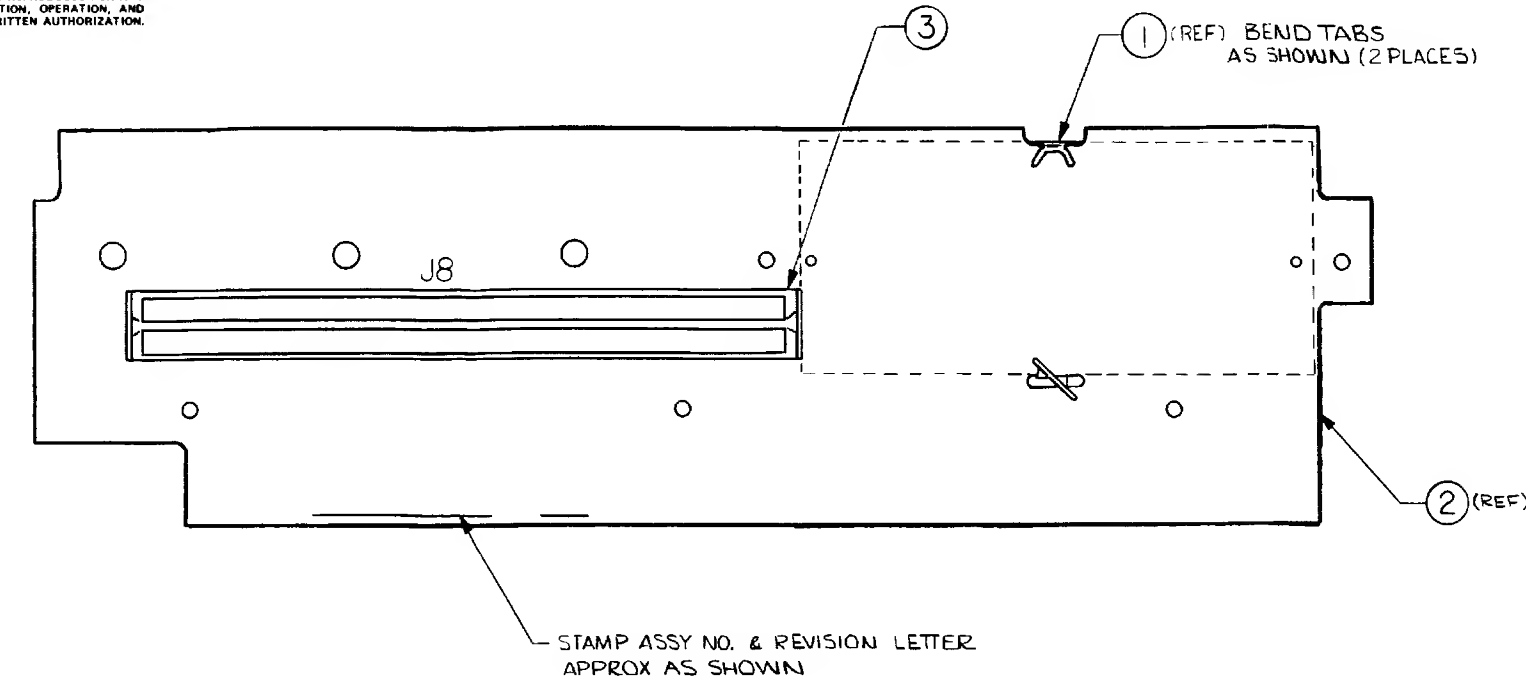

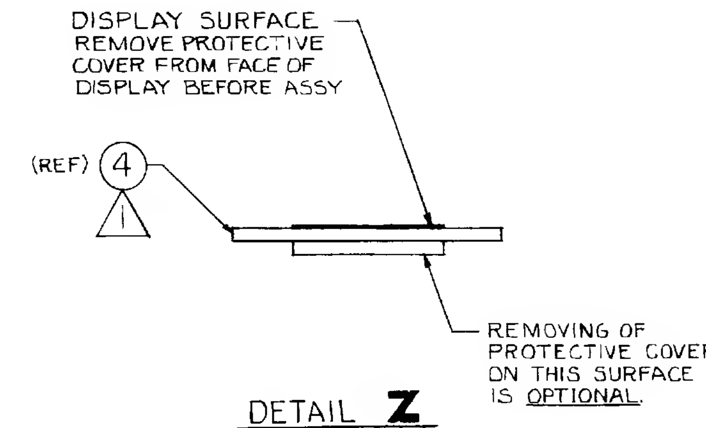

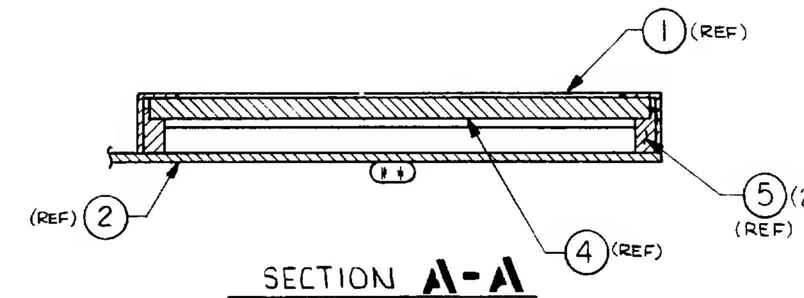

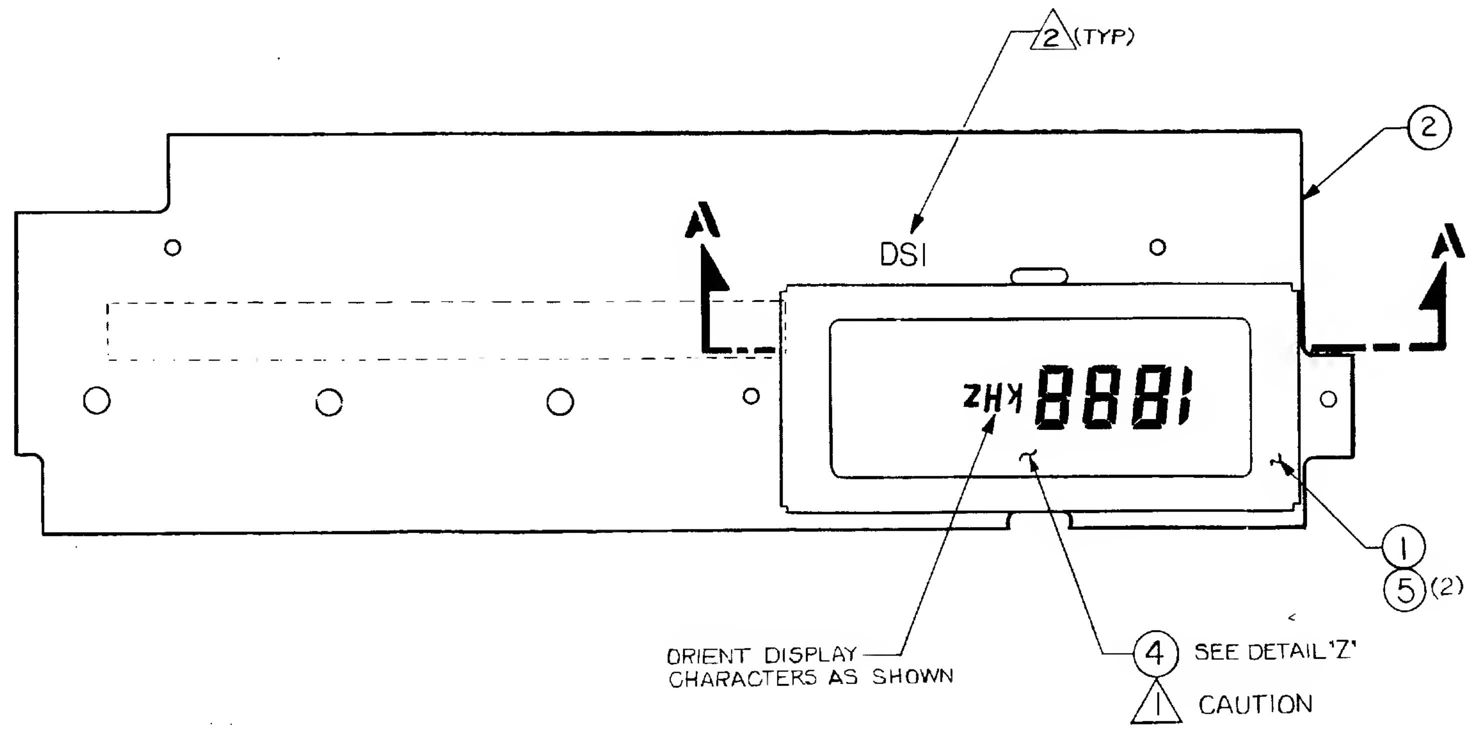

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	SCHEMATIC, DISPLAY	0103-00-1117	WVTK	0103-00-1117	1
1	BEZEL, LCD	21-6183	WVTK	1400-01-6183	1
2	DISPLAY BD	21-1117	WVTK	1700-00-1117	1
3	CONNECTOR(70 PIN)	ETC35DRTN	SULIN	2100-02-0140	1
4	DISPLAY, LCD	2400-03-0012	WVTK	2400-03-0012	1
5	LCD CONNECTOR	09191-09	TECNT	2400-03-0013	2

WAVETEK PARTS LIST — TITLE: DISPLAY BD 21-1112 — ASSEMBLY NO 1208-00-1117 — REV A — PAGE 1

4. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.

3. SEE 0103-00-1117 FOR SCHEMATIC.

2. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1A1, REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.

1. CAUTION GLASS: LCD DISPLAY IS EXTREMELY FRAGILE. CARE MUST BE USED AS NOT TO CRACK GLASS DISPLAY.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. MAGNOLIA	DATE 6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	12-14-83	TITLE PCA, DISPLAY (A1A1)
	RELEASE APPROV	11/4/83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 .XX ± .030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 21 / 22 — DWG NO 1208-00-1117 — REV A
	SCALE 2:1		CODE IDENT 23338 — SHEET 1 OF 1

1208-00-1117 A

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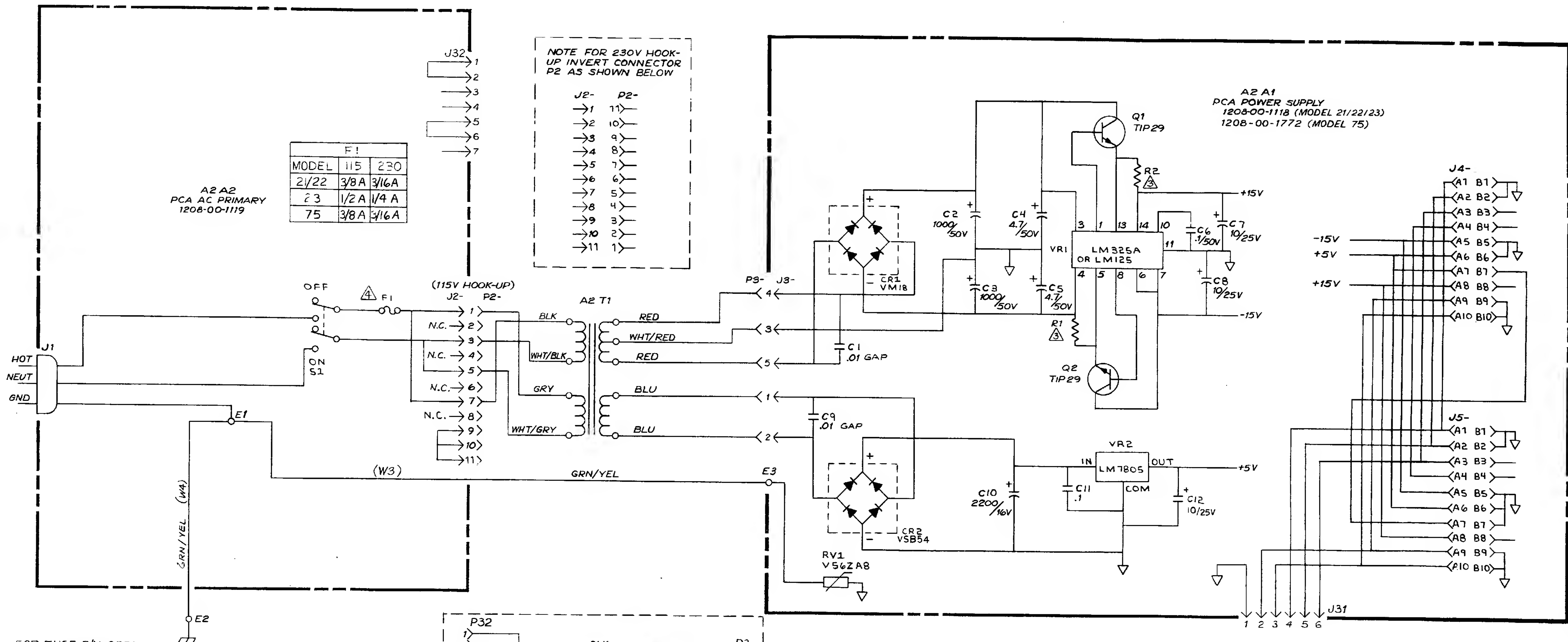
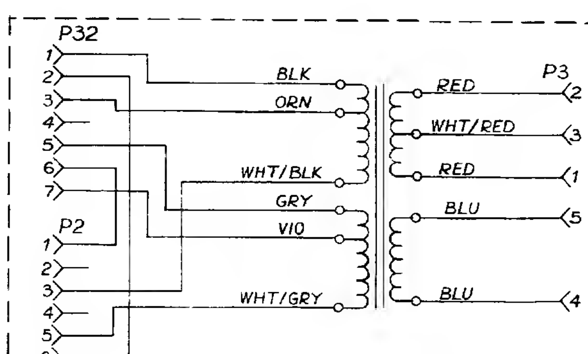
REV	ECN	BY	DATE	APP
B	# 4668, 4707	A.T.	3/4/85	
C	#4728	KA	9/10/85	
D	#6028		2/1/86	
E	#7577	A.T.	7/1/86	
F	#7695		9/15/86	
G	#7784		11/21/86	



F1		
MODEL	115	230
21/22	3/8 A	3/16A
23	1/2 A	1/4 A
75	3/8 A	3/16A



CONNECTIONS FOR TRANSFORMER WITH HI/LO AND 115/230V PRIMARIES

(SHOWN IN 115V, HI POSITION - REVERSE P32 FOR LO POSITION)

⚠4 FOR FUSE P/N SEE:
MODEL 21/22 - 1101-00-1113
MODEL 23 - 1101-00-1703
MODEL 75 - 1101-00-1771

⚠3 R1 AND R2 VALUES:
0.51Ω, 1.3 W (MODEL 21/22/23)
1.5Ω 1/2 W (MODEL 75)

2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 5/3/82
MATERIAL	PROJ ENGR	11/4/82
FINISH WAVETEK PROCESS	RELEASE APPROV	11/4/83
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1	
	DO NOT SCALE DWG	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, POWER SUPPLY (A2)

MODEL NO	DWG NO	REV
21/22	0103-00-1113	G
CODE IDENT 23338	SHEET 1 OF 1	

0103-00-1113 G

REV	ECN	BY	DATE	APP
A	ECN 4562	KA	3/27/85	
B	#4802			
C	#4881			
D	#6028	DAM	2/1/86	ACT
E	#7459	TT	9-25/86	ACT
F	7999		4 87	
G	8325	NC	12/8/87	ACT.
H	9222		9 88	
J	89-134 BOM	BG	7 27 89	KA

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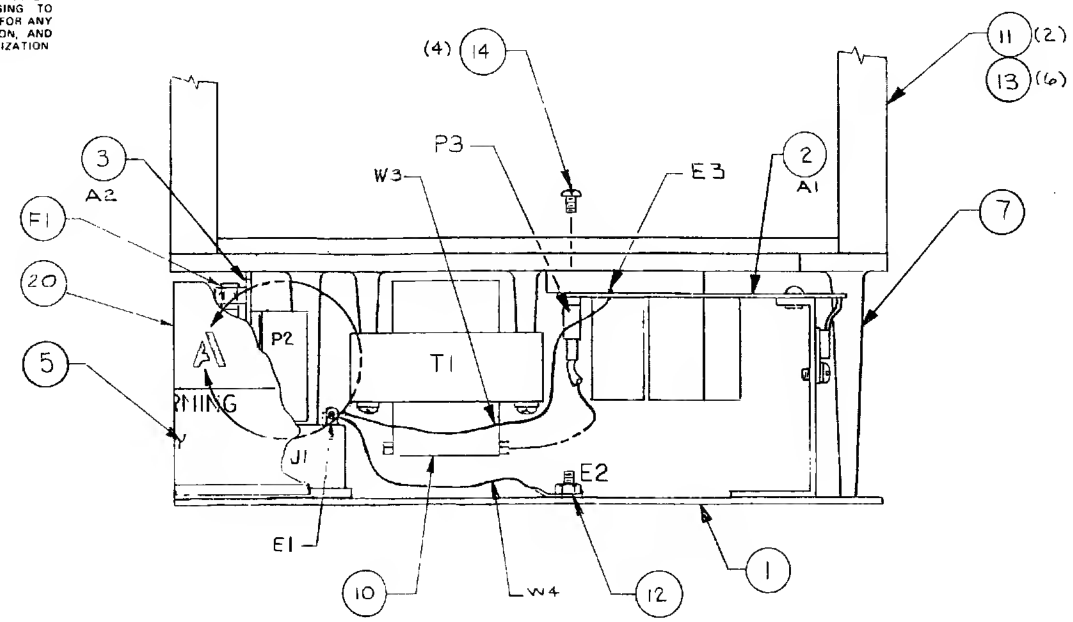
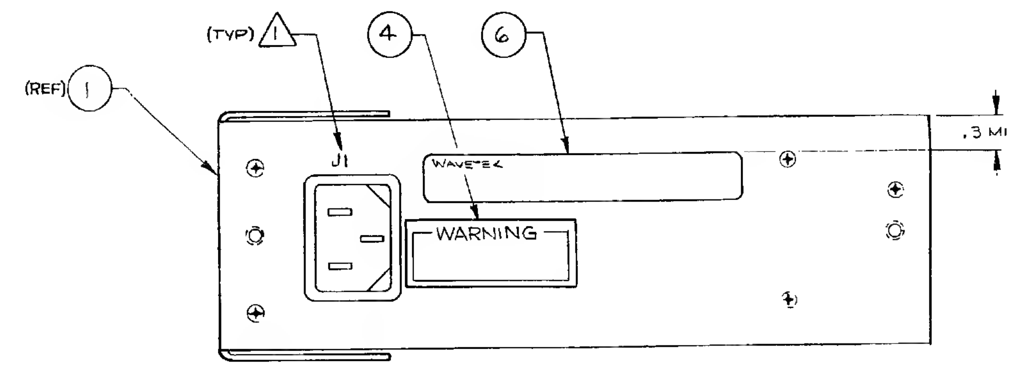
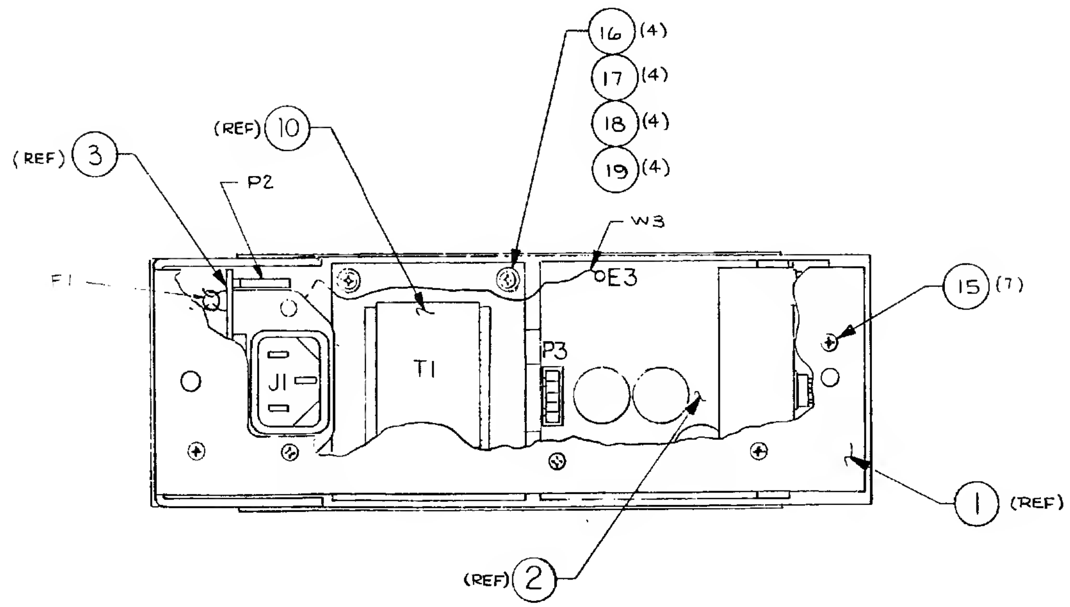
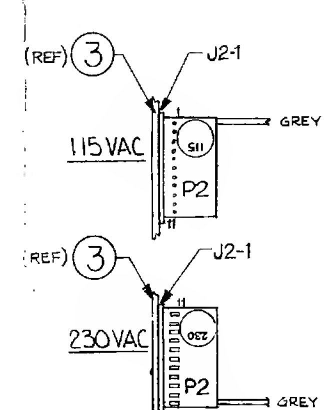




LABEL INSTALLATION



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
10	TRANSFORMER	1204-00-0061	ENSIG	1204-00-0061	1
2	PCA, POWER SUPPLY	21-1118	WVTK	1208-00-1118	1
3	PCA, AC PRIMARY	21-1119	WVTK	1208-00-1119	1
4	LABEL, WARNING	801-6940	WVTK	1400-00-6940	1
5	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
6	LABEL, SERIAL #/RATING	182A-4610	WVTK	1400-01-4610	1
NONE	LABEL, 115 VAC	21-6900	WVTK	1400-01-6900	1
NONE	LABEL, 230 VAC	21-6910	WVTK	1400-01-6910	1
20	COVER, FUSE	1400-01-8183	WVTK	1400-01-8183	1
NONE	PANEL, REAR	1400-01-8193	WVTK	1400-01-8193	1
11	PANEL, SIDE-23 (GPIB)	23-8463	WVTK	1400-01-8463	2
7	PANEL, POWER SUPPLY	1400-02-2080	WVTK	1400-02-2080	1
F1	FUSE, 3/8A, 250V, S-B	313.375	LITFU	2400-05-0009	1
12	NUT, FLEXLOC, 6-32, Z	6-32 NUT F.L.	CMRCL	2800-15-6100	1
13	SCREW, SELF TAPPING TYPE B, PAN CROSS	8-18 X 1/2	CMRCL	2800-22-8208	6
14	SCREW, 4-40X1/4, PHP, NY LOCK PATCH, Z	4-40 X 1/4	CMRCL	2800-23-4104	4
16	SCREW, #6 SAE FLAT WASHER, 375 O D	6 SAE FLAT WASHER	CMRCL	2800-26-6000	4
17	WASHER, FLAT, FIBER, #6	MS35338-136	COML	2800-28-6000	4
18	SCREW, 6-32X1 1/4 PHP, Z	6-32 X 1 1/4	CMRCL	2800-38-6120	4
19	#6 LOCKWASHER, PLATED	#6SRLW	CMRCL	2800-42-6000	4
15	SCERW, F.H. 100 DEG CSK, CROSS RECESS4-40X3/8	4-40X3/8 F H	CMRCL	2800-44-4106	7



DETAIL A
P2 INSTALLATION (115VAC OR 230VAC)

4. WIRES & CABLES OBTAINED FROM CABLE KIT 1207-00-1120.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2. REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.

NOTE UNLESS OTHERWISE SPECIFIED

WIRING LIST

	FROM	TO	REF DES
	E1	E2	W4
	E1	E3	W3
DETAIL 'A' 115 VAC	P2 (1 THRU 11)	J2 (1 THRU 11)	—
DETAIL 'A' 230 VAC	P2 (11 THRU 1)	J2 (1 THRU 11)	—
	P3 (1 THRU 5)	J3 (1 THRU 5)	—

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.MAGNOLIA	DATE 6-83
MATERIAL	PROJ ENGR	10/14/83
	RELEASE APPROV	11-4-83
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030	
	DO NOT SCALE DWG	
	SCALE 1/1 & NOTED	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE ASSEMBLY, POWER SUPPLY (A2)

MODEL NO 21/22 | DWG NO 1101-00-1113 | REV J

CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REDIKUT NO A-3894

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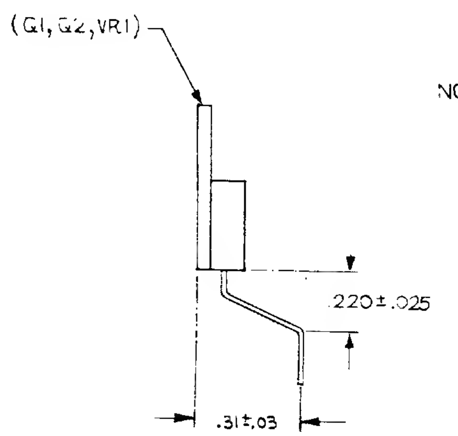
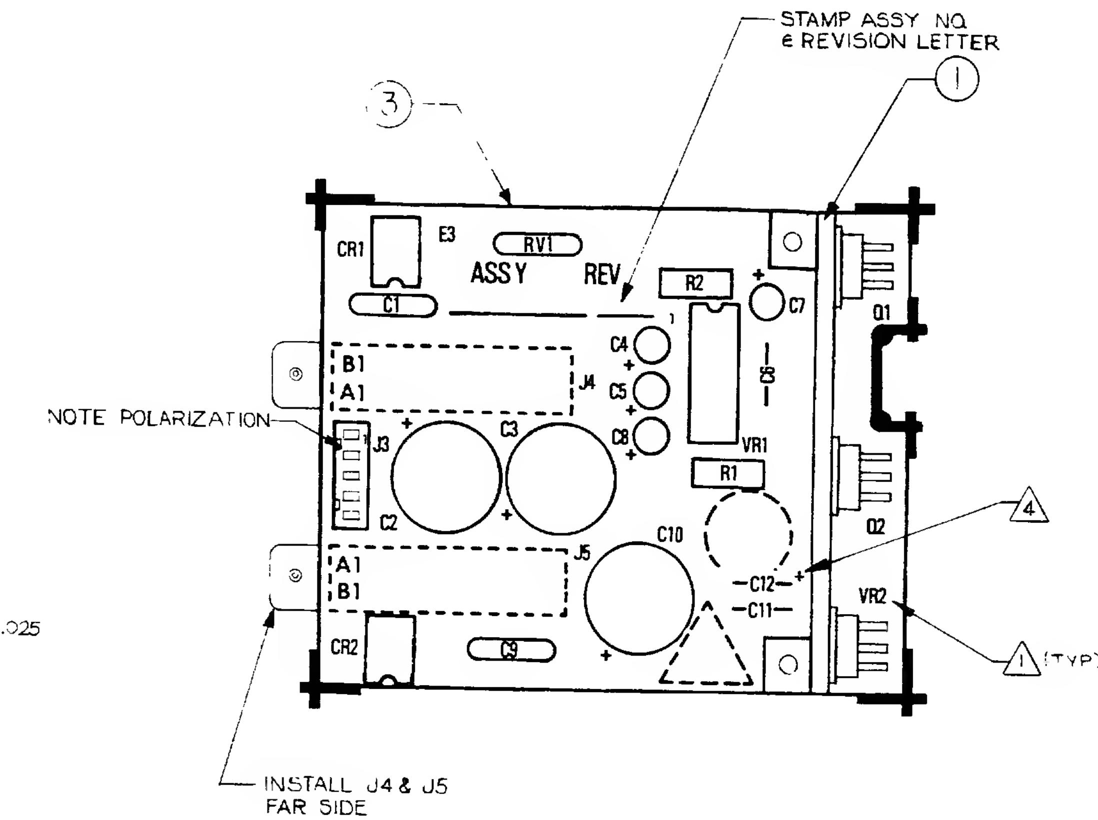
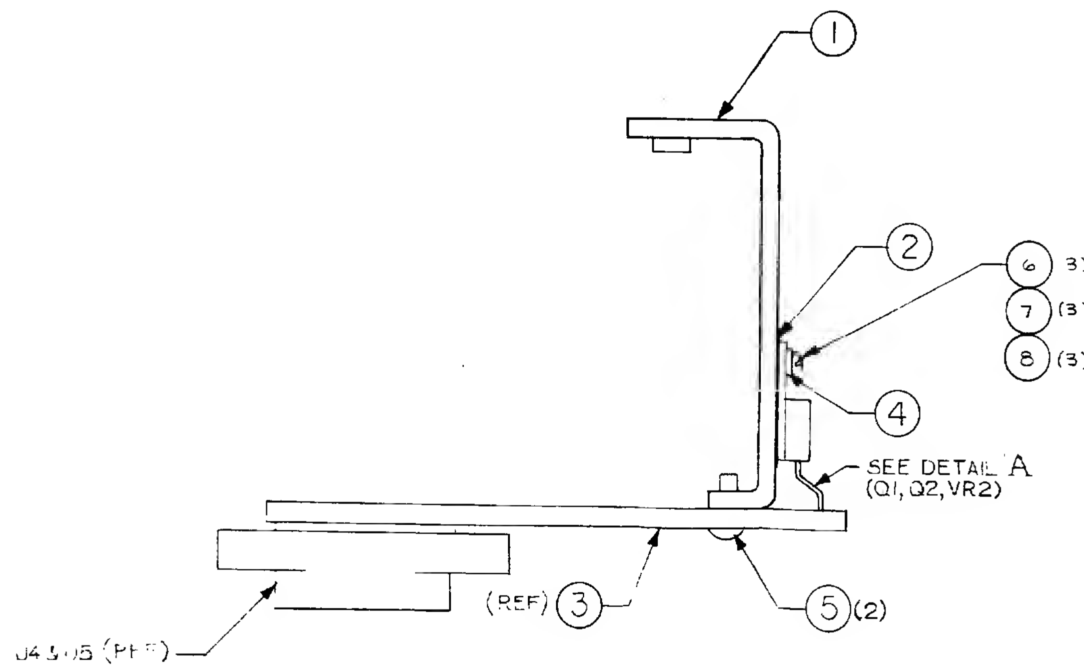
REV	ECN	BY	DATE	APP
A	4667		7/22/85	
B	#4728	KA	7/ /85	
C	#4999			
D	#7577	AT	7/11/86	
E	#7652	AT	9/24/86	
F	#7784		11/21/86	



DETAIL A
(SCALE: NONE)





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	BRKT. HEATSINK	21-8173	WVTK	1400-01-8173	1
C1 C9	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	2
C11 C6	CAP, CER, MN, .1MF, 50V, Z5U, +80/-20% RAD LD SP .2	5028ES50RD104Z	KYCRA	1500-01-0420	2
C12 C7 C8	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	3
C2 C3	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	CRE SERIES 1000/50	CAPAR	1500-31-0203	2
C10	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	CRE SERIES 2200/16	CAPAR	1500-32-2201	1
C4 C5	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	2
3	POWER SUPPLY BD	21-1118	WVTK	1700-00-1118	1
J4 J5	CONNECTOR(20 PIN)	ETCIODRTI	SULIN	2100-02-0139	2
J3	HEADER, CONN(5 PIN)	102202-2	AMP	2100-02-0143	1
4	WASHER	851547F015	MOT	2800-11-0015	3
5	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
6	SCREW, SELF TAPPING TYPE B, PAN CROSS	4-24 X 3/8	CMRCL	2800-22-4162	3
7	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	3
8	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	3
2	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	3
RV1	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
R1 R2	RES, MF, 1/2W, 5%, .51 OHM	A21-0R51J	DALE	4799-00-0144	2
CR1	DIODE, BRIDGE	VM18	VARO	4801-02-0008	1
CR2	DIODE, RECTIFIER, DUAL IN-LINE	VSB54	VARO	4806-02-0054	1
Q1 Q2	TRANS	TIP-29	TI	4902-00-0290	2
VR1	IC, VOLTAGE REGULATOR	LM325AN	NSC	7000-03-2501	1
VR2	VOLT REG	MA7805UC	FAIR	8000-78-0500	1

4. INSTALL C12 OBSERVING INDICATED POLARITY.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A1.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE 6/13/85
MATERIAL | PROJ ENGR
FINISH: WAVETEK PROCESS | RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PCA, POWER SUPPLY (A2A1)

MODEL NO 21/22 | DWG NO 1208-00-1118 | REV F
CODE IDENT 23338 | SHEET 1 OF 1

1208-00-1118 F

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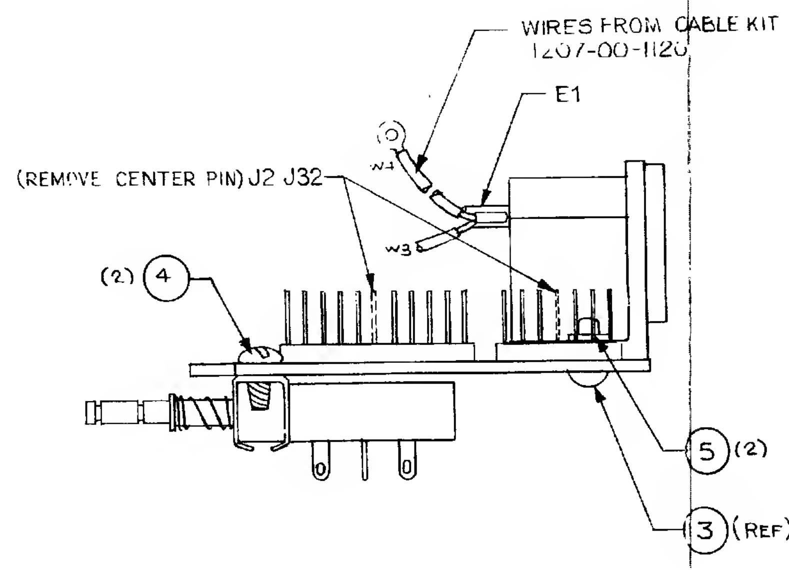
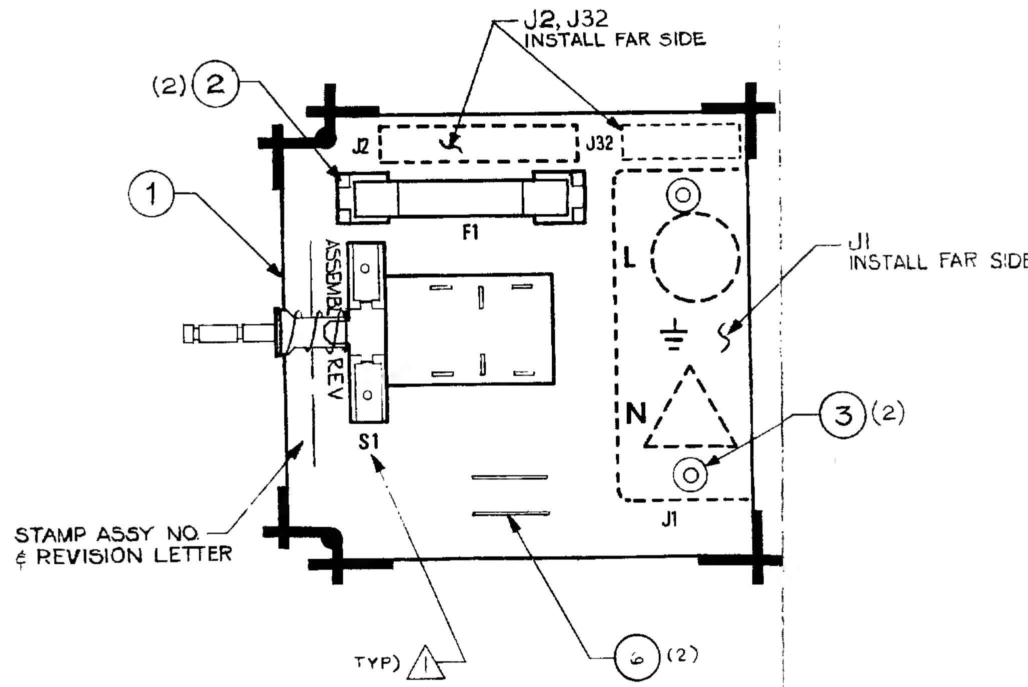
REV	ECN	BY	DATE	APP
A	#4251 4546 4250			
B	#4595			





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	AC PRIMARY BD	21-1119	WVTK	1700-00-1119	1
J2	HEADER, CONN(11 PIN)	1-87224-1	AMP	2100-02-0144	1
J32	CONN, HEADER, UNSHROUDE 0, 7 PIN	87224-7	AMP	2100-02-0184	1
J1	RECEPT, POWER(PC)	EAC-303	SWCFT	2100-03-0069	1
2	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	2
3	RIVET, ALUM 5/16X1/8 01A . 188-250	1125-0410	CHOBT	2800-12-0047	2
4	SCREW, S/T TYPE B, PAN CROSS RECESS, 4-24X1/4	4-24 X 1/4	CMRCL	2800-22-4142	2
5	WASHER, FLAT, 4(.312 O.D.)	#4FW	CMRCL	2800-26-4000	2
6	RESISTOR, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	2
S1	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A2.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

PROJ. ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ±1
XX ± .030

DO NOT SCALE DWG

SCALE 2:1

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
PCA,
AC PRIMARY
(A2A2)

MODEL NO 21/22

DWG NO 1208-00-1119

REV B

CODE IDENT 23338

SHEET 1 OF 1

1208-00-1119 B